



The New Verification Ecosystem Supporting RISC-V Verification for all Adopters



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Abstract

- The RISC-V design freedoms have enabled implementers to innovate new and creative solutions. As a design progresses from concept to completion, the flexibility of RISC-V has implications for the hardware functional verification teams
- This talk covers some of the latest developments in the RISC-V verification ecosystem to address new approaches for automating processor verification
- These include:
 - Open standards to support universal testbenches and VIP (Verification IP) reuse
 - Coverage libraries and quantitative measures for test infrastructure quality
 - Novel techniques to verify cache coherency and SoC integration
- Key Points:
 - Different RISC-V processor types & systems e.g. embedded, application, clusters have different verification needs
 - Automation is the answer, and this includes various diversified test generation technologies
 - Imperas and Breker are evolving new flows & solutions to address essential RISC-V verification ecosystem needs



- Challenges for RISC-V cores / systems verification teams
- Imperas background – simulation & verification of RISC-V cores / systems
- Breker background – automated test generation for RISC-V cores / systems
- Collaboration to provide improved RISC-V verification solutions
- Summary

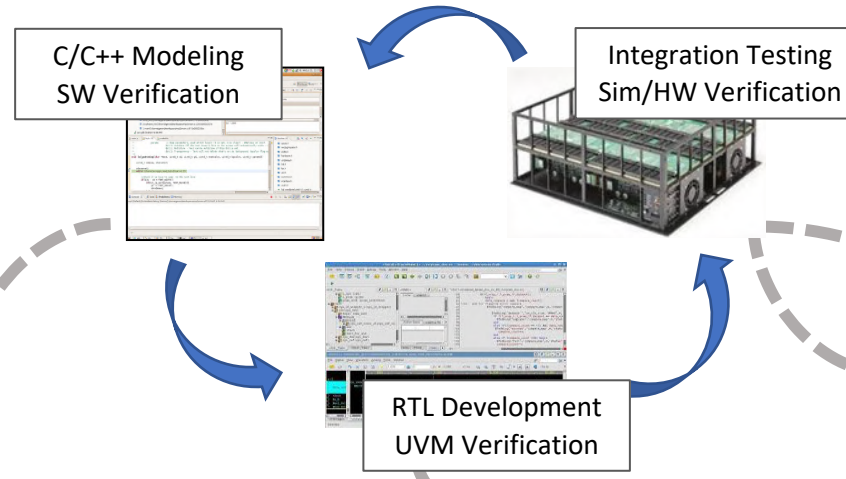
Verification challenges for RISC-V cores & systems



Processor Core Verification

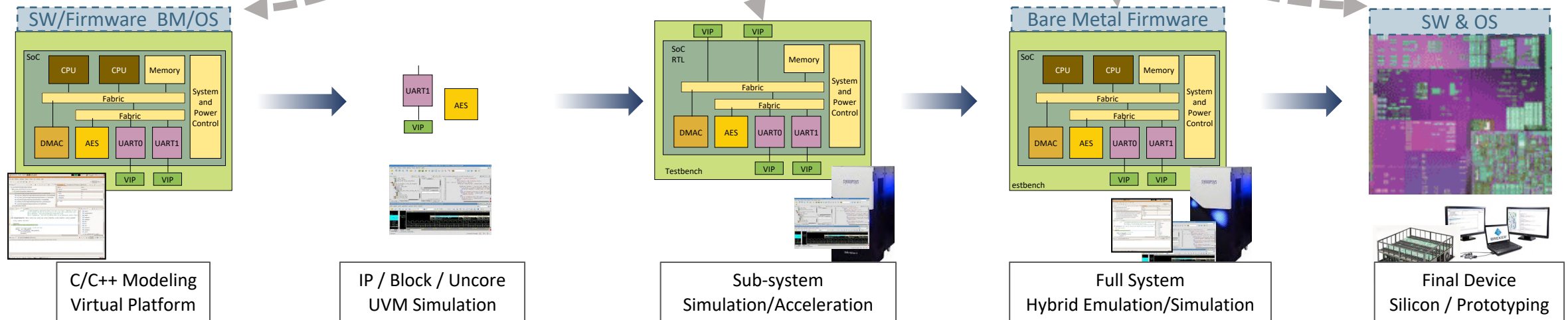
- 100% coverage, commercial grade verification necessary
- ISA compliance, in-depth micro-architecture, custom instructions
- Effective integration capability & performance

Processor Core Verification



SoC Verification and Validation

- Processor to SoC function and performance compatibility
- SoC infrastructure (e.g., coherency, security)
- Uncore, processor & platform combined functional testing



SoC Verification and Validation



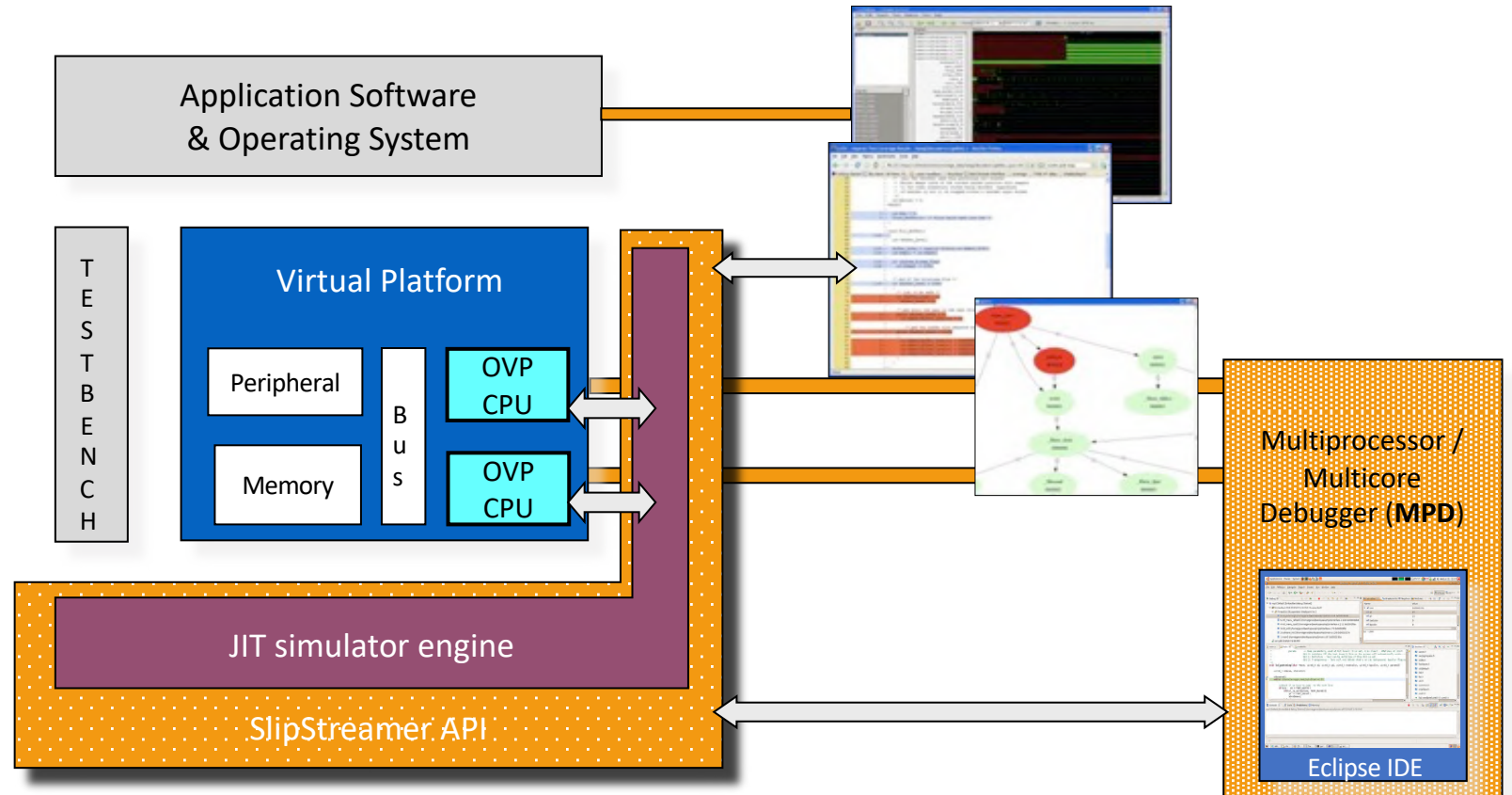
Agenda

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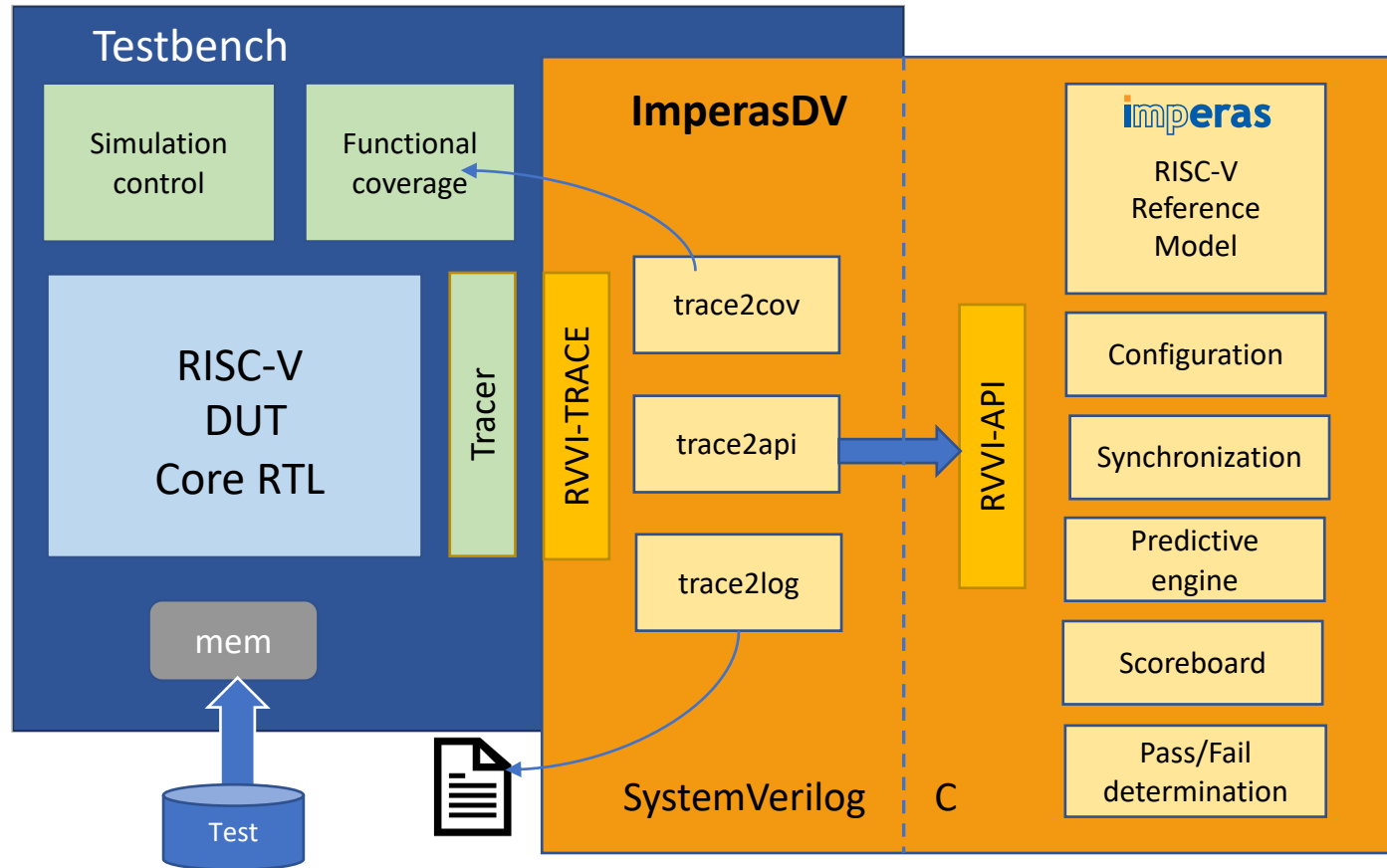
Imperas Environment for Embedded Software Development, Debug & Test

Key technologies/differentiators:

- OVP Fast Processor Models
 - Most models (Arm, RISC-V, MIPS, ...)
 - Highest quality
- Simulator engine
 - Highest performance
 - SlipStreamer API for non-intrusive tools
- Tools
 - MPD for platform-centric debug
 - VAP tools for comprehensive software analysis
 - Trace, profile, coverage, etc.



ImperasDV: 'Out-of-the-box' RISC-V Processor DV Solution



- Built on RVVI
 - Open standard
 - RVVI-TRACE
 - RVVI-API
- Re-usable VIP for DV of RISC-V processors
 - Single, multi-hart
 - In-order, out-of-order
 - Single, multi-issue
 - Custom instructions
 - Un-privilege ISA
 - Privilege ISA
 - Debug & Hypervisor
- Async-lock-step-compare
- C/C++/SystemVerilog
- Includes needed DV components
- Works with all leading RTL simulators
- Easy to use: For each core...
 - Create tracer
 - Configure Imperas reference/VIP

Imperas: The RISC-V simulation leader



- Involved with RISC-V International since 2016
 - Active in Formal/Golden model, Compliance, many ISA extensions, & other working groups
 - Shipped first reference model of RISC-V core in 2017
 - Imperas RISC-V golden reference models used for DV since 2018
- Founding member of the OpenHW Group – commercial quality open-source RISC-V IP cores
- The most complex RISC-V projects use Imperas:
 - Nvidia Networking (Mellanox), Nagravision, AMD, NXP, Silicon Labs, Dolphin Design, EM Micro US (Swatch), NSITEXE (DENSO subsidiary), Top-tier systems company (AI application) , Startup building accelerator based on multiprocessor RV64, Japanese government projects “TRASIO” and “RVSPF”, Numerous universities around the world, 150+ organizations using free riscvOVPsimPlus, ...
- Many partnerships in RISC-V verification ecosystem:
 - OpenHW, Chips Alliance, Google (open source ISG), Breker (test synthesis), Valtrix (test generation tools), Andes (processor IP vendor), SiFive (processor IP vendor), Cudasip (processor IP vendor), MIPS (processor IP vendor), Imagination (processor IP vendor), Microchip (Microsemi FPGA Mi-V processor IP), Intel (Nios-V for FPGA), Intel (Pathfinder IDE), ...

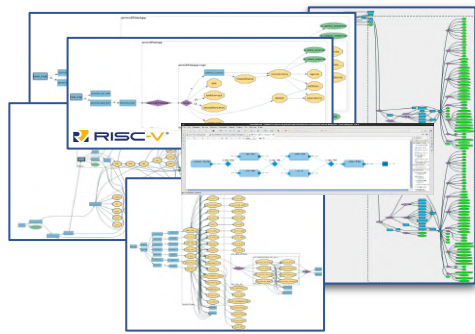
Simulation & Verification of RISC-V Cores / Systems



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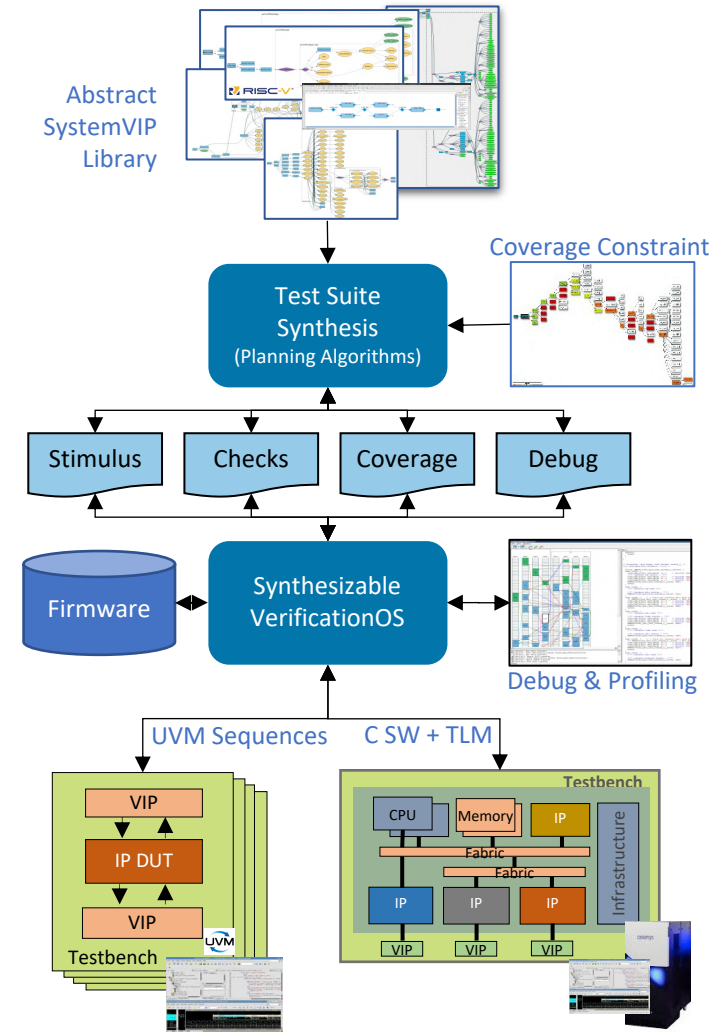
Breker Background: Test Suite Synthesis for RISC-V Cores & SoCs

- Breker is a key, longstanding part of the verification ecosystem for processors and SoCs based on x86 and Arm architectures
- Breker has become part of the verification ecosystem for processors and SoCs based on RISC-V architectures
 - Working with multiple RISC-V developers and users/integrators
- RISC-V has room to grow if we solve the verification barrier
 - We are experienced in x86 and Arm verification, allowing us to share this experience with RISC-V teams through automated tests

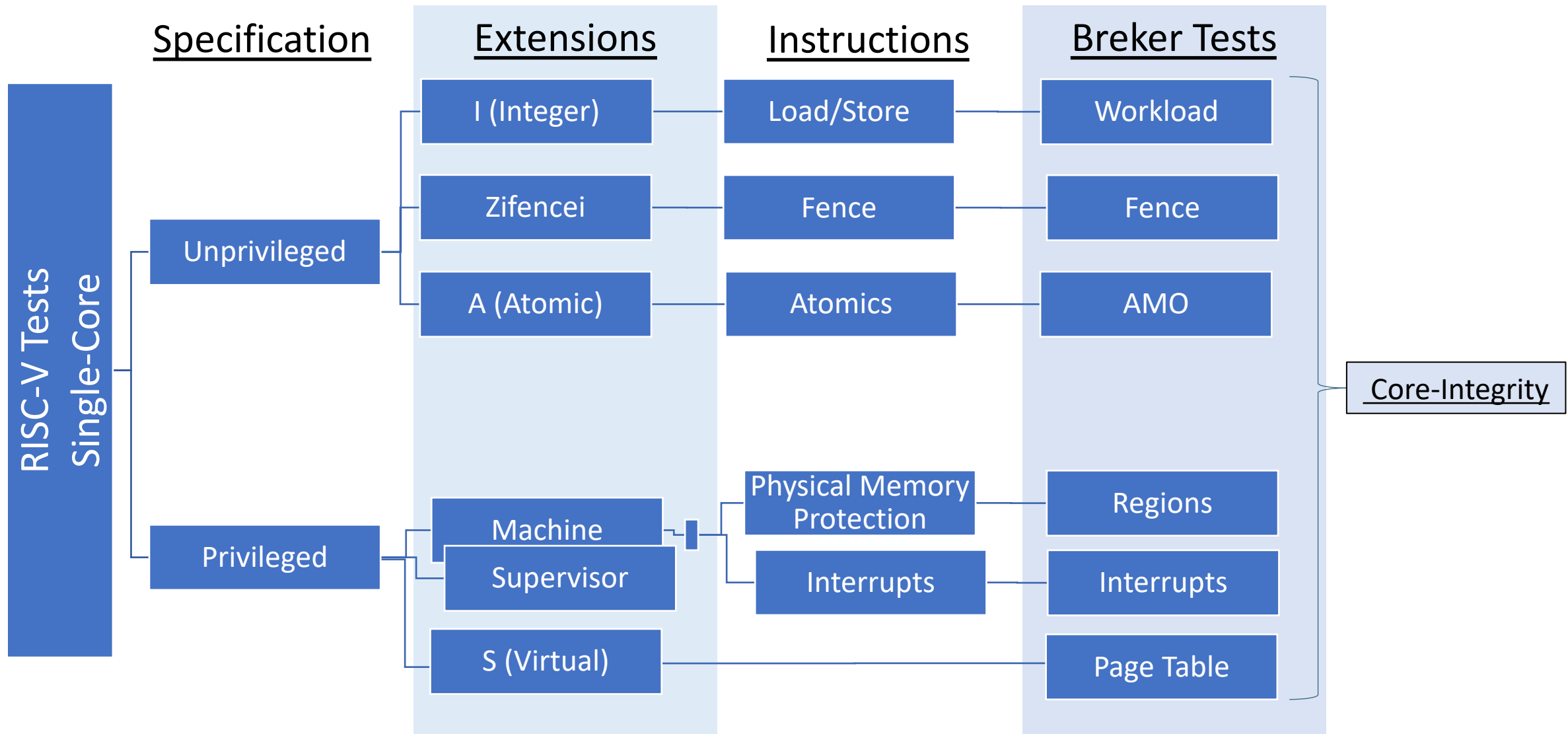


The Breker SystemVIP Library

- Core Integrity FastApps
- RISC-V System Integrity TrekApp
- ARM System Integrity TrekApp
- Cache Coherency TrekApp 2.0
- Firmware-First TrekApp
- Power Management TrekApp
- Security TrekApp
- Networking TrekApp



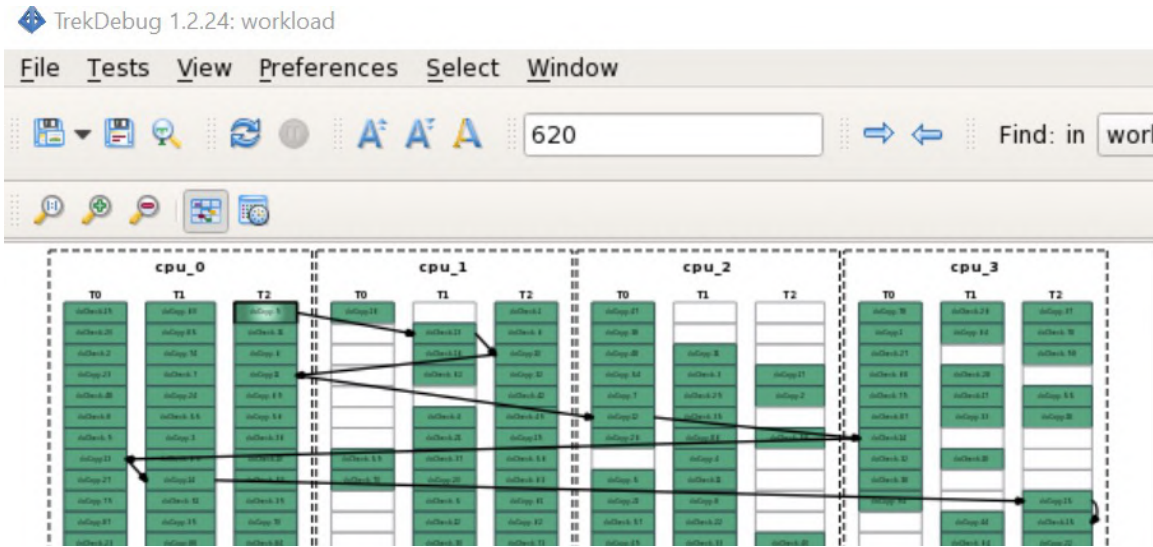
Breker Core-Integrity FastApp RISC-V Test Generation



Core-Integrity Example: Multi-Hart (x4), 3 Threads Each

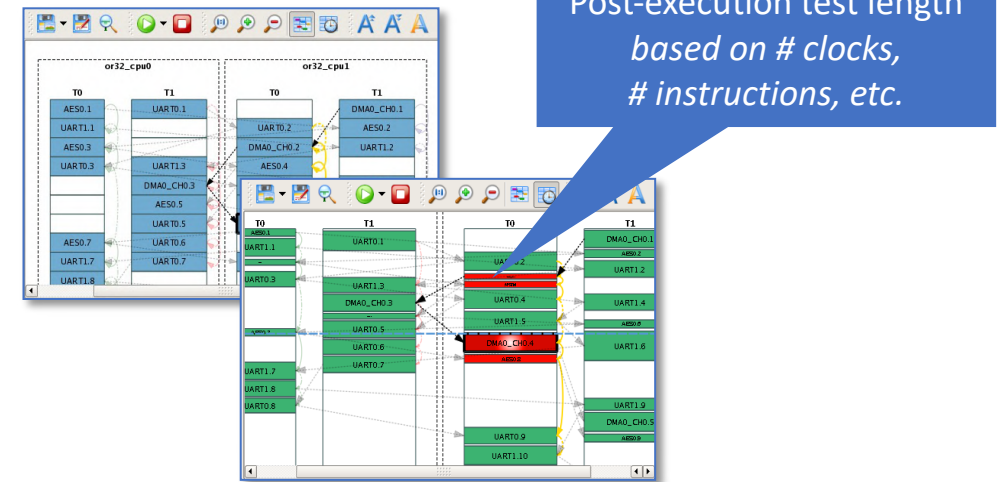
Breker Concurrent Scheduling Stress Tests the Processor/SoC

Advanced, Abstract Debug



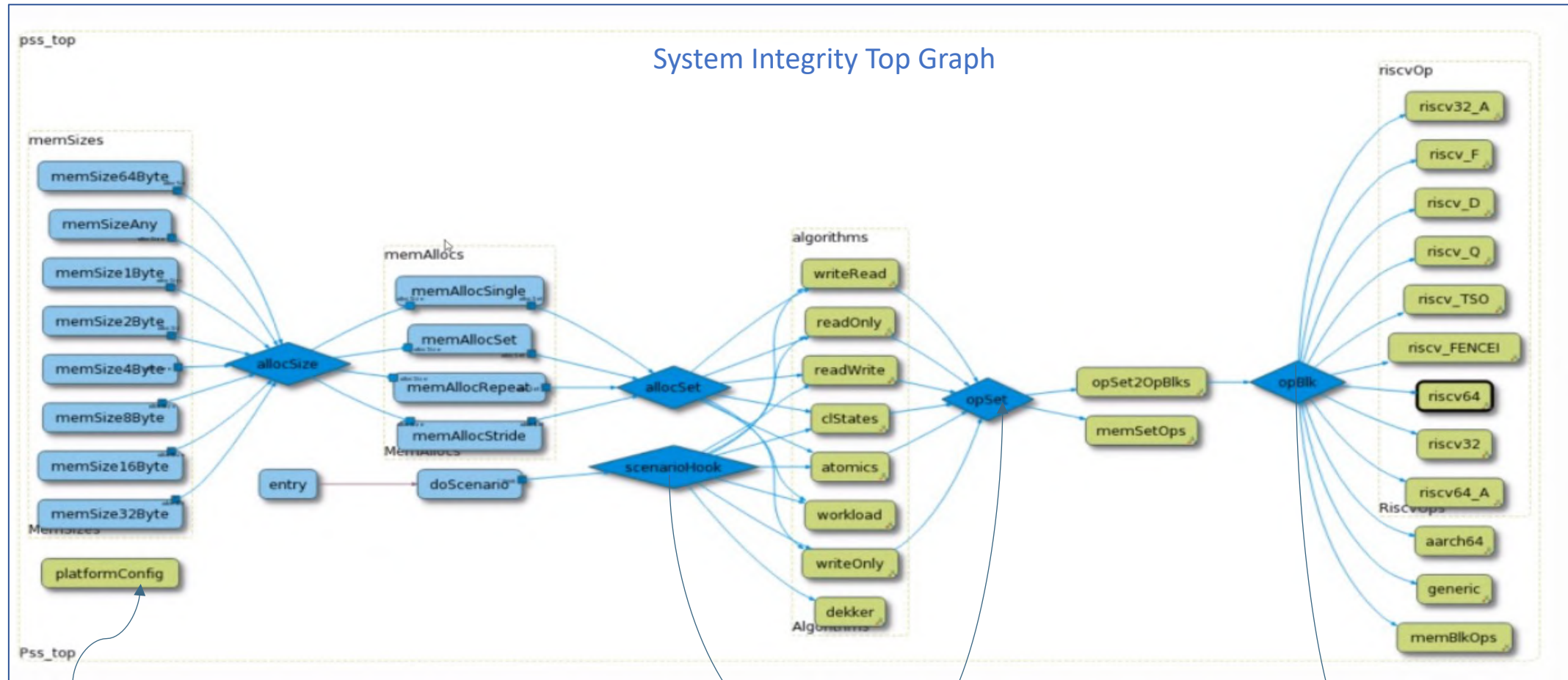
Quickly observe concurrent multi-test progress and DUT reaction

Execution Profiling



Post-run analysis of design performance/power bottlenecks

Modular, Configurable, Extendable VIP



Max Memsize
 ADD: Specific Component Characteristic

Specialized Algorithm
 ADD: Special Coherency Test Algorithm

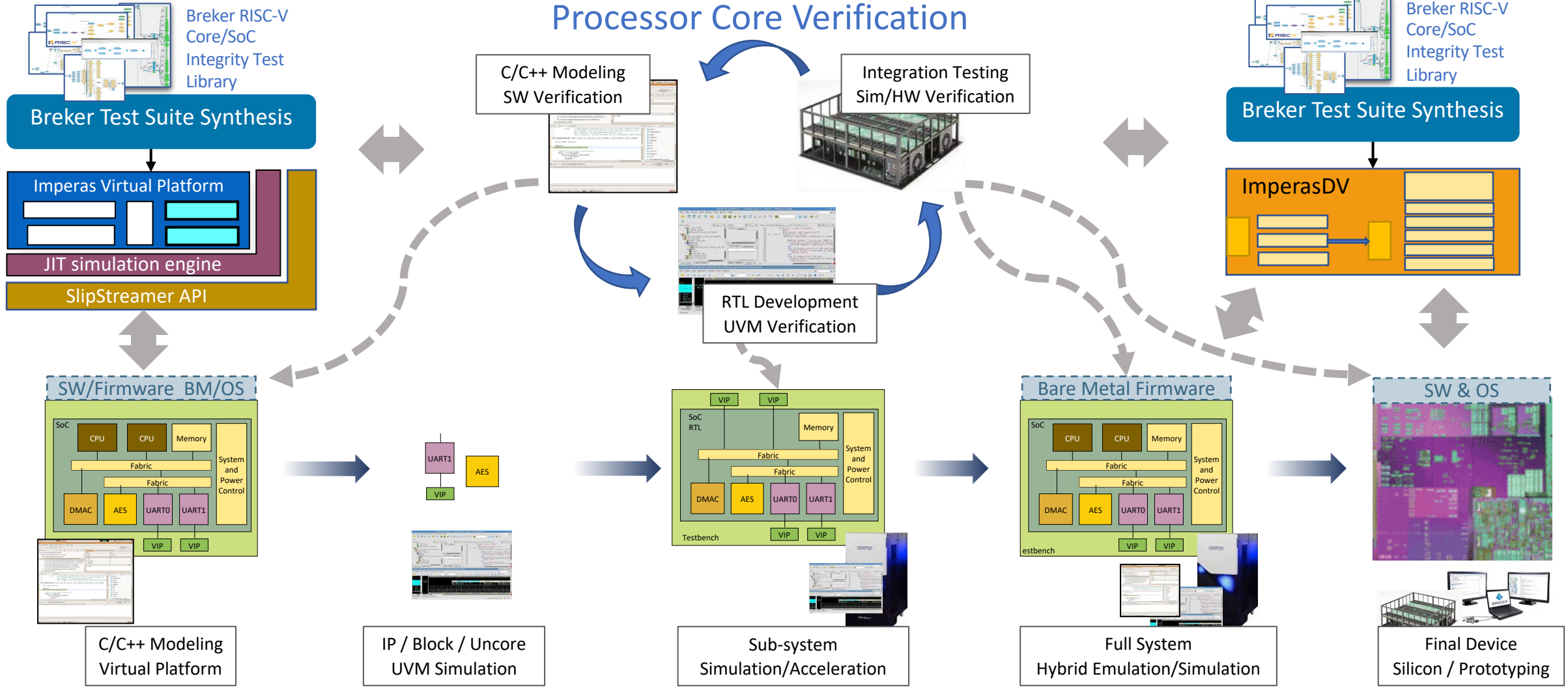
Custom Instructions
 ADD: Extra Processor Instruction

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Imperas/Breker RISC-V Multi-level Partnership



Processor Core Verification



SoC Verification and Validation



RISC-V verification challenges addressed by Imperas/Breker work

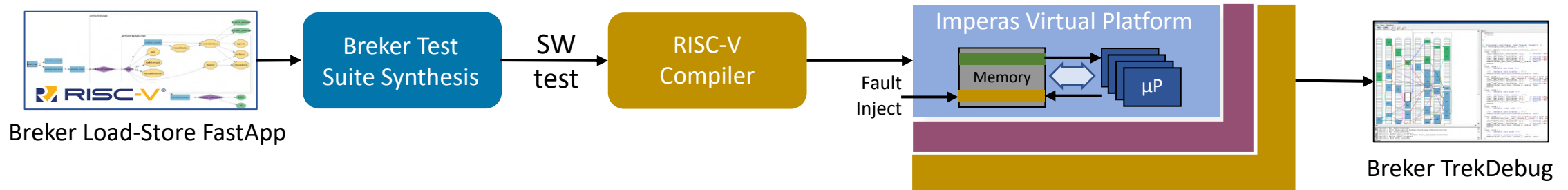


- Single core privilege mode test generation & quality verification:
 - Interrupts
 - PMP memory accesses
 - MMU/virtual memory
 - Breker “Core-integrity”
 - ImperasDV verification and fault injection
- SoC Integration test generation – with graph based end-to-end test creation:
 - Multi-hart / multi-core memory accessing
 - Cache / NOC memory hierarchy coherency checking
 - Breker “System-integrity”
 - Imperas virtual platform simulation with fault injection
- Allows the measuring of testing quality and corner case coverage



Example Verification Test

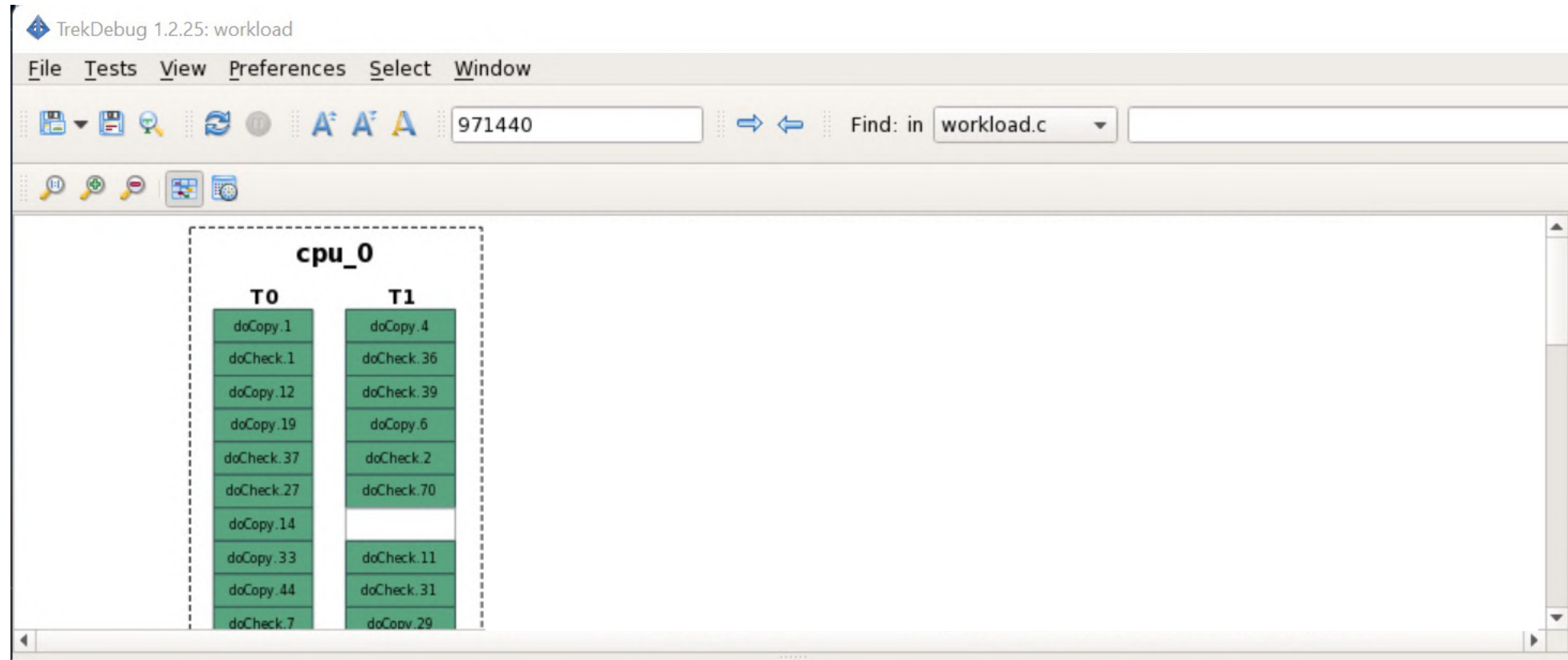
Note: Simple Test for Fast Demonstration Purposes



- Example DUT: 64-bit RISC-V 4 core with external memory
- Simple load-store test example: data consistency on transfer
- Breker load-store integrity FastApp on Imperas Virtual Platform / Simulator
 - Compiled SW test running bare metal on core
- Inject fault to create bug for demo purposes, check profile, etc.

TrekDebug GUI

Observe Concurrent Scheduling Test-Progress



TrekDebug 1.2.25: workload

File Tests View Preferences Select Window

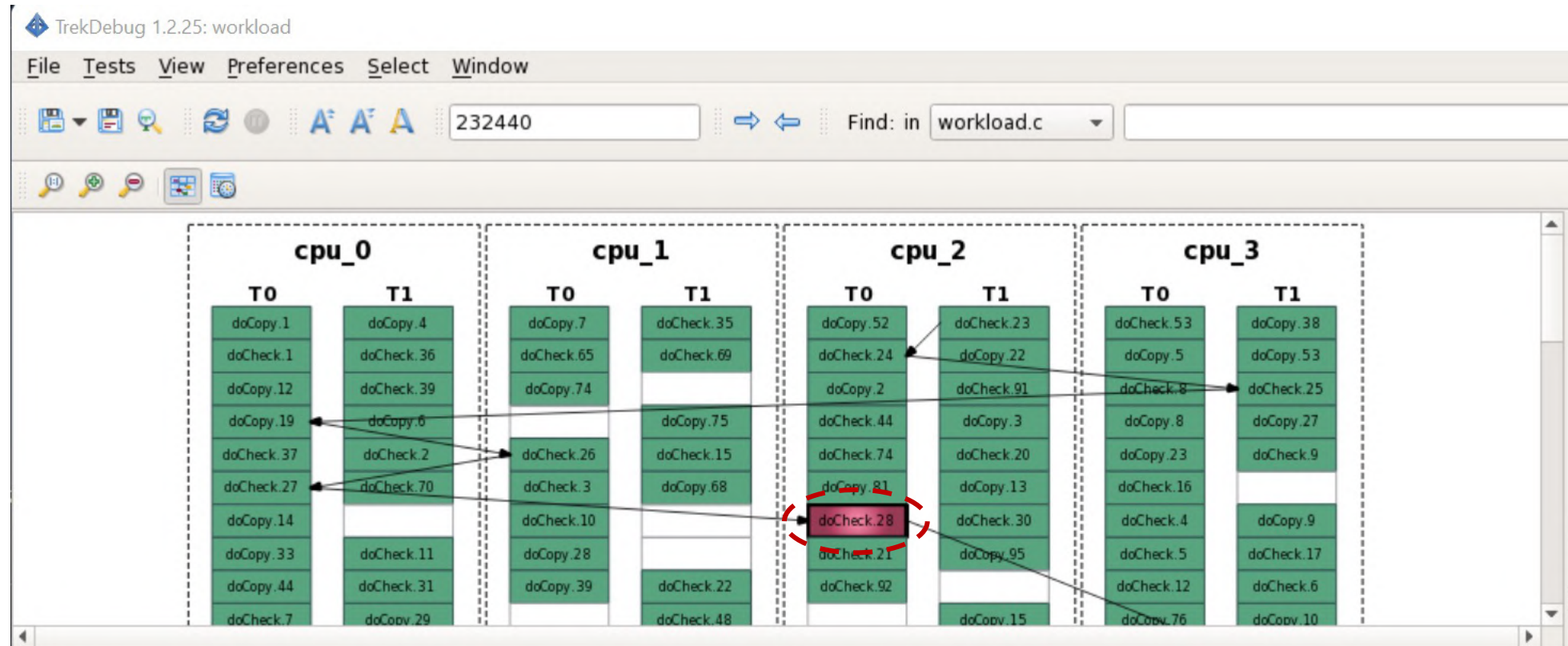
971440 Find: in workload.c

cpu_0

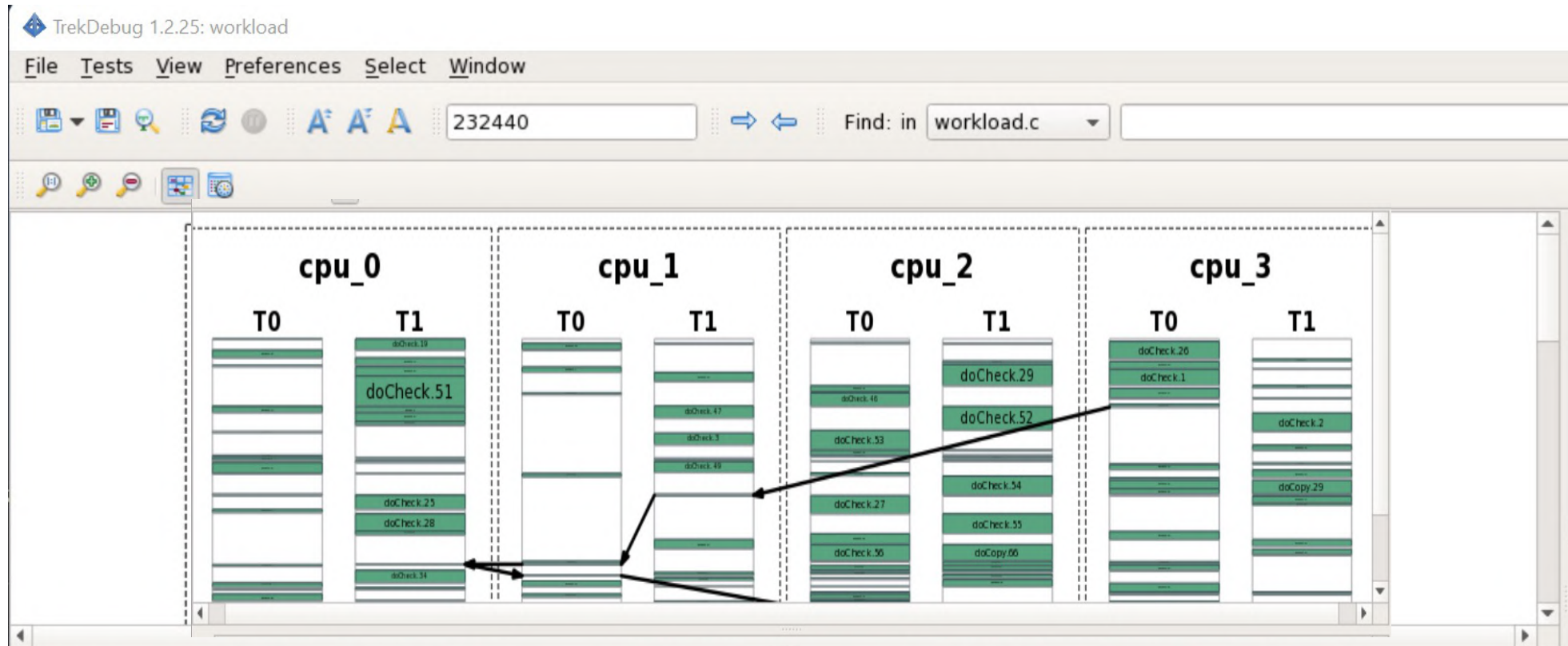
T0	T1
doCopy.1	doCopy.4
doCheck.1	doCheck.36
doCopy.12	doCheck.39
doCopy.19	doCopy.6
doCheck.37	doCheck.2
doCheck.27	doCheck.70
doCopy.14	
doCopy.33	doCheck.11
doCopy.44	doCheck.31
doCheck.7	doCopy.29

TrekDebug GUI

Observe Failing Test-Segments



TrekDebug – Execution Profiling (based on instruction-count)



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Summary



- RISC-V has enormous, transformational potential, but commercial grade verification is critical and cannot be ignored
 - Disconnect between:
 - Processor IP quality out-of-the-box industry perception
 - The extreme complexity of ensuring across the board processor quality
- Automation required to achieve \$100M-per-year Arm verification excellence
 - Most processor providers cannot make this level of investment
 - Automation enables these verification processes across the industry
- Imperas and Breker: decades of experience in this field with many processor/SoCs
 - Developers can raise quality levels by leveraging experience of many verification projects
 - Integrators can gain confidence in their processors by ensuring they drive SoCs correctly

For More Information: imperas.com brekersystems.com

