Imperas Newsletter – Feb. 2023

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The leader in RISC-V simulation solutions

Headline Story

BREAKFAST BYTES

Improving RISC-V Processor Quality with Verification Standards and Advanced Methodologies

At the RISC-V Summit in December, there were presentations halfway between a keynote and a technical session known as RISC-V Spotlights. These were presented to the entire group of attendees but were not blessed with the keynote title. Maybe this is like the way that when a physician in Britain becomes a surgeon, they drop the title "Dr." and go back to "Mr.". A spotlight is even better than a keynote. One spotlight was by Simon Davidmann of Imperas titled Improving RISC-V Processor Quality with Verification Standards and Advanced Verification Methodologies…

To read the full **Breakfast Bytes** article by **Paul McLellan**, click here.

Also, watch the spotlight talk by **Simon Davidmann** at: https://youtu.be/CojvlnbGD-A

Videos

Larry Lapides, Vice President Sales at Imperas Software, interview with **Calista Redmond** at RISC-V Summit 2022.

Upcoming Events

SemIsrael Tech Webinar, February 14 2023

Imperas will present at SemIsrael Tech Webinar, the virtual event featuring presentations on the latest updates for the design and development of semiconductor ICs and SoCs.

RISC-V Models for Verification, Architectural Exploration, and Software Development

This talk highlights the RISC-V models that are unifying the hardware, software, and verification teams across all phases of RISC-V projects with dependable quality and efficiency.

Speaker: Larry Lapides – Imperas Software
When: Tuesday, February 14, 2023 – 4:30pm (Israel Time Zone)

You can follow this link for more information about the SemIsrael Tech Webinar and free registration.

RISC-V Webinar with Andes and Imperas, February 23, 2023

RISC-V custom extensions offer new freedoms to optimize a processor to the requirements of the target application.

RISC-V Design Innovations with Custom Extensions

A 'software first' design flow incorporating virtual-platforms / virtual-prototypes, allows SoC developers to explore new hardware configuration options with the application software workload and full OS supports. This webinar will feature updates from Andes and Imperas with highlights from use cases and examples across market segments for IoT, 5G, and AI/ML.

When: Thursday, February 23, 2023 - 09:30am (PST)

To register for this webinar, please follow this link.

DVCon, February 27 to March 2, 2023

Imperas will participate at DVCon 2023 in San Jose, presenting a joint conference paper with OpenHW, an in-depth tutorial on the latest simulation-based RISC-V processor verification techniques, plus a booth (#108) in the expo hall with the opportunity to chat 1-1 with the Imperas team.

Conference paper:

The Evolution of RISC-V Processor Verification: Open Standards and

Verification IP

This paper will describe the evolution of RISC-V processor verification methodology using CORE-V-VERIF as a case study. The current generation uses RISC-V processor verification IP enabled by the open standard RISC-V Verification Interface (RVVI) to realize a comprehensive verification methodology that encompasses asynchronous peripheral events that occur randomly during program execution.

Co-authors: Aimee Sutton, Imperas Software
Lee Moore, Imperas Software
Mike Thompson, OpenHW Group

When: Tuesday, February 28th – 3:00pm (PST)

Workshop:

Understanding the RISC-V Verification Ecosystem

This workshop will help the audience understand and navigate the RISC-V verification ecosystem. Some of the topics covered include:

- Understanding the tools used in RISC-V processor verification: instruction set simulators, processor reference models, random instruction stream generators, verification IP
- Compare and contrast techniques that can be used for RISC-V processor verification: post-simulation trace compare, self-checking tests, lockstep co-simulation, functional coverage
- Open standards for RISC-V processor verification: RISC-V Verification Interface (RVVI)
- Open-source examples and commercial offerings

Presenters: Aimee Sutton, Imperas Software
Simon Davidmann, Imperas Software

When: Thursday, March 2nd – 1:30pm to 3:00pm (PST)

For more information about Imperas's participation in the event, please follow this link. To arrange a 1-to-1 appointment during DVCon 2023, please email us at: info@imperas.com

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Embedded World Exhibition and Conference, March 14-16 2023

Imperas will be at Embedded World 2023 in Nuremberg, Germany, demonstrating solutions for RISC-V processor verification, software development with virtual prototypes and extensions with custom instructions in conjunction with debug and analysis tools and solutions to accelerate embedded software development. Imperas are co-sponsors of the RISC-V Pavilion located in Hall 4A stand 4A-620 and will also participate in the following talks:

Conference Paper:
Advanced methodologies to address RISC-V verification for all adopters
Speaker: Jon Taylor – Imperas Software
Co-authors: Mike Thompson – OpenHW Group
Kevin McDermott – Imperas Software
Simon Davidmann – Imperas Software
Lee Moore – Imperas Software
When: Wednesday, March 15, 2023: Session 9.2 – 2:15pm (CET)

Conference Paper:
New ecosystem leads RISC-V mainstream adoption with innovation ready software development and processor verification tools
Speaker: Larry Lapides – Imperas Software
Co-authors: Mike Thompson – OpenHW Group
Davide Schiavone – OpenHW Group
Kevin McDermott – Imperas Software
Simon Davidmann – Imperas Software
When: Thursday, March 16, 2023: Session 9.3 - 12:00pm (CET)

Conference Paper:
Example of Extending RISC-V for AI/ML Domain Specific Processors
Speaker: Larry Lapides – Imperas Software
Co-authors: Pascal Gouedo – Dolphin Design
Damien Le Bars – Dolphin Design
Olivier Montfort – Dolphin Design
Mike Thompson – OpenHW Group
Kevin McDermott – Imperas Software
Lee Moore – Imperas Software
Aimee Sutton – Imperas Software
When: Thursday, March 16, 2023: Session 9.3 - 4:00pm (CET)

RISC-V Theatre:

Introduction to RISC-V Processor Verification

Speaker: Larry Lapides – Imperas Software
Where: RISC-V Pavilion in Hall 4A stand 4A-620
When: Tuesday, March 14, 2023: 10:30am (CET)

RISC-V Theatre:

Getting started with RISC-V custom instructions

Speaker: Jon Taylor – Imperas Software
Where: RISC-V Pavilion in Hall 4A stand 4A-620
When: Wednesday, March 15, 2023:10:00am (CET)

Stop by the RISC-V Pavilion (Hall 4A stand 4A-620) to see all the latest Imperas simulation technology for RISC-V, including advanced RISC-V processor verification, virtual prototypes, software development and custom instruction, plus support for the latest ratified RISC-V specifications including vector accelerators and draft extensions included with the Imperas reference model for RISC-V.

For more information, please follow this link, or to set up meetings with Imperas at the Embedded World 2023, please contact: info@imperas.com

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Articles

Solutions Disclosed at RISC-V Summit: Security, Verification, and More

At this year's RISC-V Summit, stakeholders rolled out solutions revolving around verification, security, and software-defined SoCs...

To read the full **All About Circuits** article by **Jake Hertz**, click here.

ARTICLES FROM SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

Selecting the right RISC-V Core

Ensuring that your product contains the best RISC-V processor core is not an easy decision, and current tools are not up to the task...

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

Design And Verification Methodologies Breaking Down

As chips become more complex, existing tools and methodologies are stretched to the breaking point...

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

Release Information

riscvOVPsim and riscvOVPsimPlus - LATEST NEWS

The latest Imperas and OVP release at the Open Virtual Platforms website.

Open Virtual Platforms

For an introduction to RISC-V the free single-core envelope model, called **riscvOVPsim**, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the latest ratified specifications including Bit Manipulation, Crypto (scalar) and Vectors.

The latest version is available via GitHub here.

The free enhanced **riscvOVPsimPlus**, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the OVPworld website here.

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