Imperas Newsletter – January 2021

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RISC-V Reference Model for Processor DV

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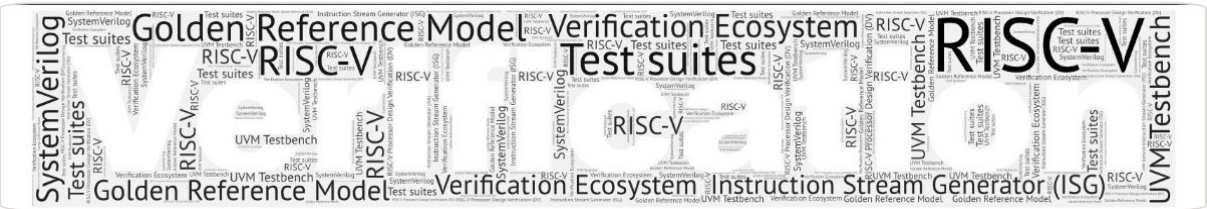
Latest news



Imperas Leads The RISC-V Processor Verification Ecosystem

Verification IP extended with Floating-Point architectural validation test suites based on golden reference model and coverage-based development

Imperas announces the latest addition to the Imperas RISC-V Verification IP (VIP) solutions with the Floating-Point architectural validation test suites covering the RISC-V Specifications for 32bit Single-Precision (**32F**), 64bit Single-Precision (**64F**), and 64bit Double-Precision (**64D**). These tests extend the current Imperas range of tests for ratified and near-ratified specifications tests, and complement the de facto industry adoption of the Imperas RISC-V verification reference model.

Processor verification is the essential focus of any development team. Design bugs that are caught early help projects complete on schedule and provide timely solutions to the target market.

The latest RISC-V verification ‘step-and-compare’ methodology can be used to verify an RTL processor implementation against the Imperas golden reference model encapsulated within a SystemVerilog UVM environment. This covers asynchronous events and offers a seamless, time-saving, transition to debug analysis when an issue is found. More details on test benches with Imperas

RISC-V verification reference models are available from the Imperas website.

To help developers ensure their processor designs meet the RISC-V specifications, Imperas has developed an instruction stream test generator for directed-tests and is now making many architectural validation test suites available.

Suites totalling over 3.5 million instructions now available for free as open-source. The free **riscvOVPsimPlus** package, including the test suites and functional coverage analysis, are now available on OVPworld. The riscvOVPsimPlus solution is an entry ramp for development and verification and includes a proprietary freeware license from Imperas, which covers free commercial use as well as academic use. The simulator package also includes a complete open-source model licensed under the Apache 2.0 license.

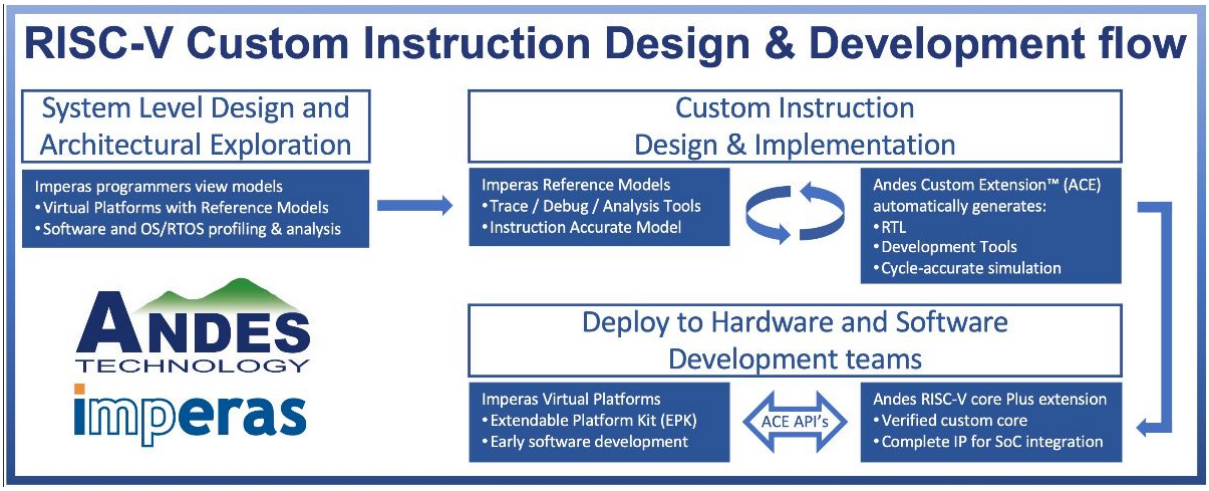
Read more

I'm ready to book a demo

Events

Webinar: RISC-V Custom Instructions – Design, Development and Deployment Feb 24 2021

Imperas and Andes are co-hosting a webinar on optimising a RISC-V processor with custom instructions and extensions for domain-specific SoCs addressing the biggest opportunities in new markets such as IoT, AI, or 5G.



Register for webinar

Imperas at the virtual DVCon, March 1-4 2021

Online virtual event on the latest advances for RISC-V Verification with RISC-V Processor Reference Models and Verification IP

Presentation: Jump start your RISC-V project with OpenHW
Imperas joined by **OpenHW Group**, **Futurewei**,
Silicon Labs and **EM Microelectronic**

Presentation: 'RISC-V Processor Verification: Case Study'
Imperas joined by **NVIDIA Networking**

Panel discussion on Verification In The Open-Source Era
moderated by Brian Bailey, Semiconductor Engineering

Imperas joined by **SmartDV**, **DARPA**, **Mentor**, **Axiomise** and **Google**

Preview our presentations

Imperas at virtual Embedded World, March 1-5 2021

Imperas participating at the online virtual digital event with the latest updates for RISC-V Verification and SoC Architecture Exploration for AI applications with virtual platforms.

Join Simon Davidmann for a live presentation titled ‘Software driven SoC Architectural Exploration for AI and ML accelerators with RISC-V' at the EW2021 Technical Conference

Learn more

Articles

SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

The Lost Art Of Processor Verification

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Using SoC methodologies for RISC-V processor DV.

JANUARY 4TH, 2021 - BY: **KEVIN MCDERMOTT**

View the article

Additional articles from SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

Multicore Debug Evolves To The System-Level

Complexity is making this process more difficult, but new and better approaches are being developed. Read more.

Stretching Engineers

The role of engineers is changing, and they need to be picking up new skills if they are to remain valuable team players. There are several directions they could go in. Read more.

RISC-V Verification Challenges Spread

Continuous design innovation adds to verification complexity, and pushes more companies to actually do it. Read more.

Release information

OVP and riscvOVPsim RELEASE NEWS

The latest Imperas and OVP release at the Open Virtual Platforms website.

For an introduction to RISC-V the free single core envelope model, called riscvOVPsim, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the draft specifications for Bit Manipulation and Vectors.

The latest version was uploaded on 24 December 2020, Version: 20201224.0 and is available via GitHub here.

The free enhanced riscvOVPsim, including the RISC-V Vector test suite, is now available on the OVP website here.

riscvOVPsim, learn more

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