A Common Software Development Environment for Many-core RISC-V based Hardware and Virtual Platforms

RISC-V 7th Workshop – Barcelona
Tuesday May 08, 2:00pm

Simon Davidmann – Imperas Software
Gajinder Panesar – UltraSoC

Agenda

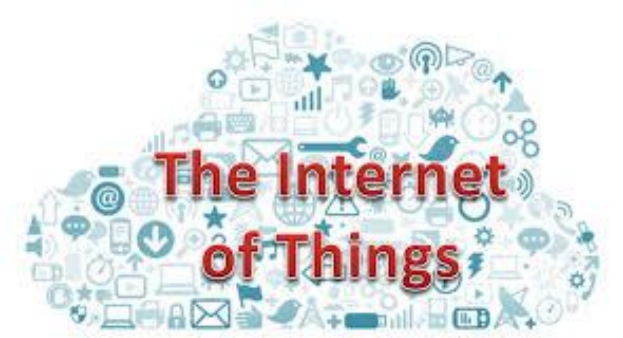
- Embedded Software Development Challenges
- Traditional SW Debug Environment using Hardware
- Modern SW Debug using Imperas Simulation
- Giving more visibility to SW Debug using UltraSoC Hardware
- Imperas/UltraSoC collaboration provides common solution

Agenda

- Embedded Software Development Challenges
- Traditional SW Debug Environment using Hardware
- Modern SW Debug using Imperas Simulation
- Giving more visibility to SW Debug using UltraSoC Hardware
- Imperas/UltraSoC collaboration provides common solution

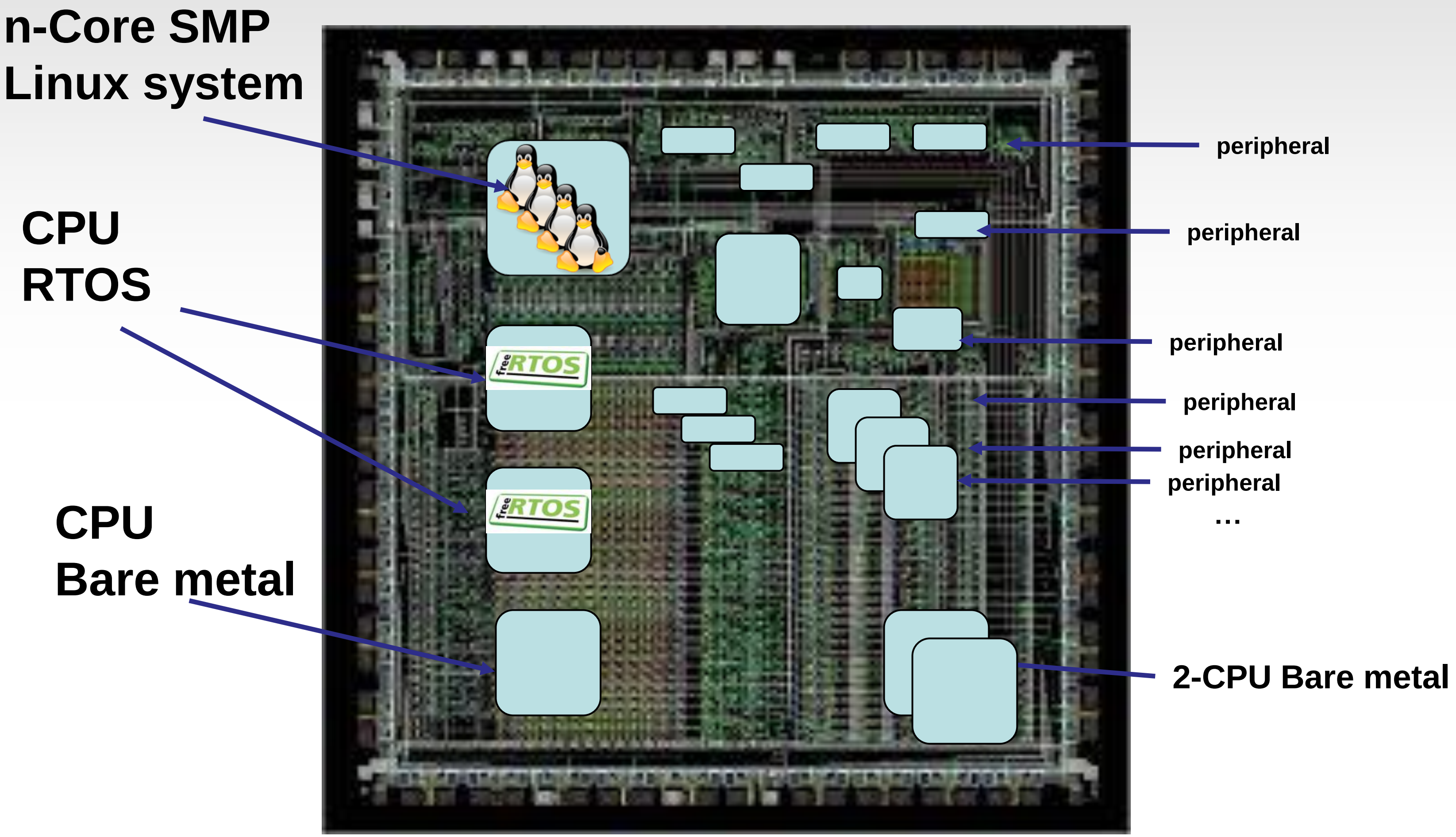
New Markets with new Software Requirements

- Schedule
- Quality
- Reliability
- Security
- Safety



- Engineering productivity / automation
- Predictability on software development schedules
- Unknown / unmeasurable software delivery risk

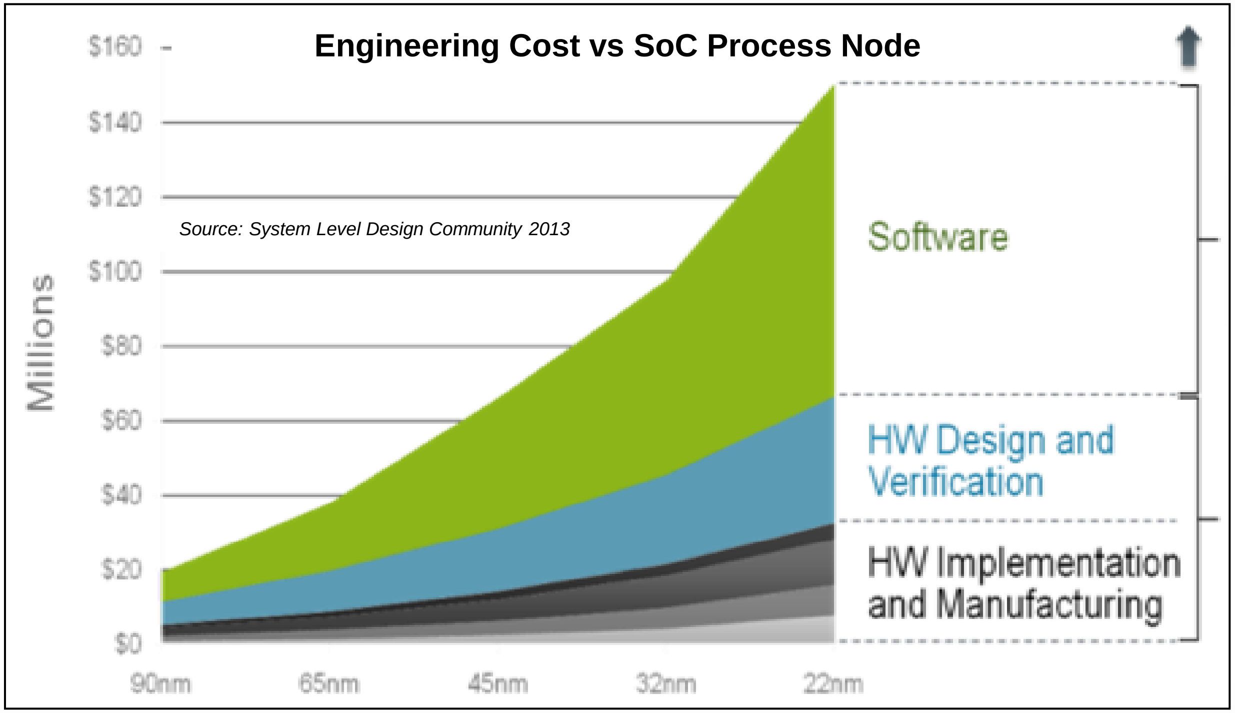
Chip designs get more complex inc. Asymmetric Multi-Core…



- Example… SMP CPU groups, AMP CPU, many peripherals and other processors…

Embedded Software Increasingly Important & Engineering Intensive

- Functionality of SW is defining embedded products
- SW codebase size, complexity, quality requirements exploding
- Engineering schedules & costs under pressure and harder to manage

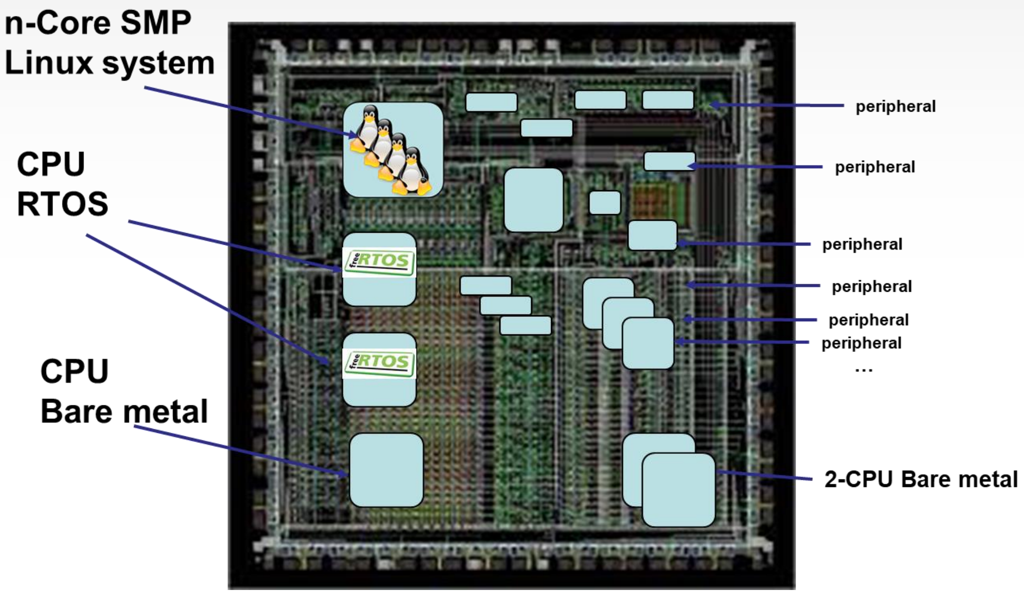


Source: System Level Design Community 2013

Agenda

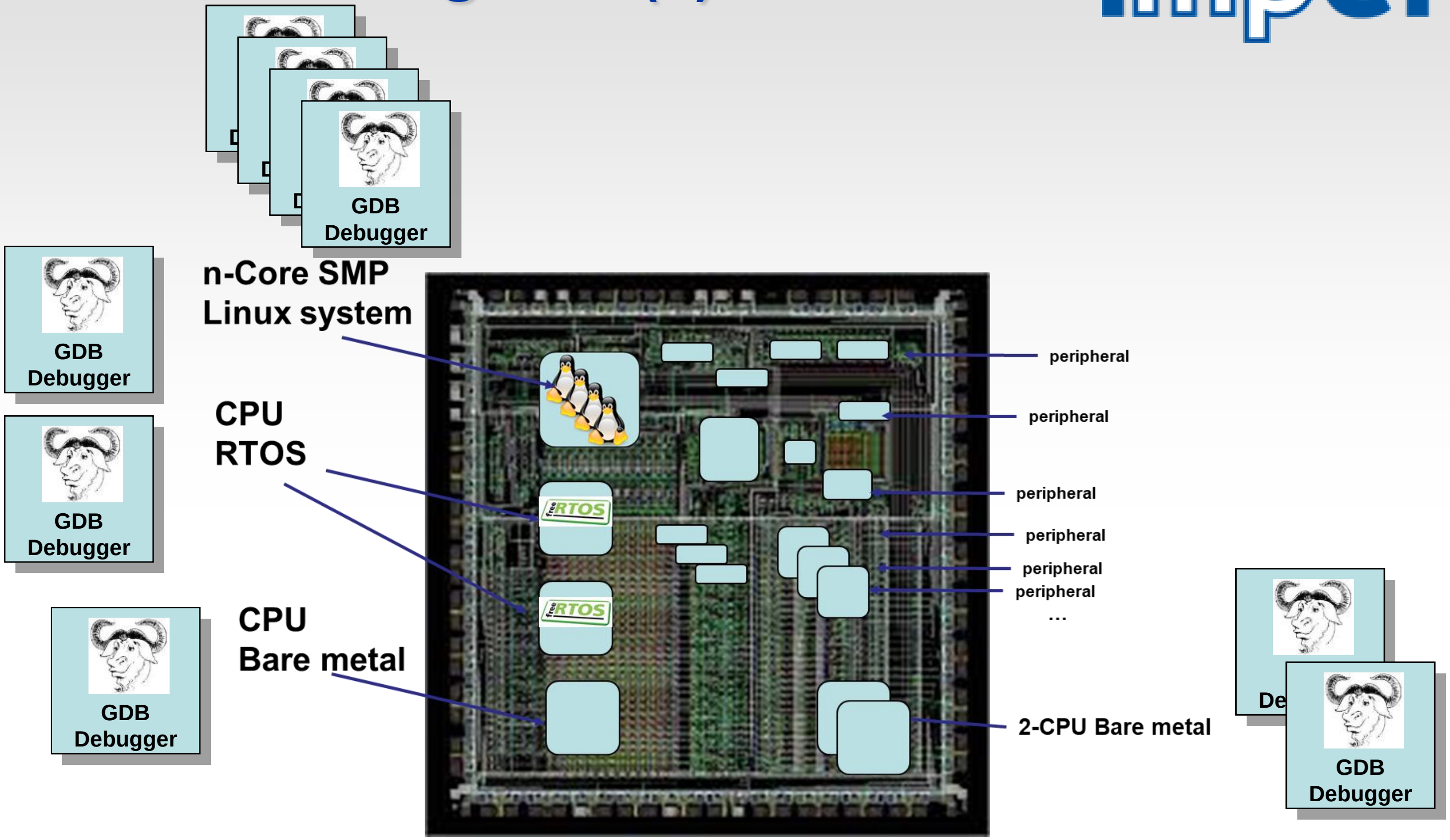
- Embedded Software Development Challenges
- Traditional SW Debug Environment using Hardware
- Modern SW Debug using Imperas Simulation
- Giving more visibility to SW Debug using UltraSoC Hardware
- Imperas/UltraSoC collaboration provides common solution

Traditionally use a hardware breadboard… Using GDB(s)…



Well.. You use one GDB per processor with JTAG giving access…

Traditionally use a hardware breadboard… Using GDB(s)…



- one GBD per CPU
- little visibility: each GDB only sees the limited memory space of the attached CPU
- non-deterministic (bugs move around…)
- poor control (hard to set specific places to break)
- scheduling and synchronized events difficult to reproduce…
- what is going on in the peripherals? …
- pretty un-manageable…

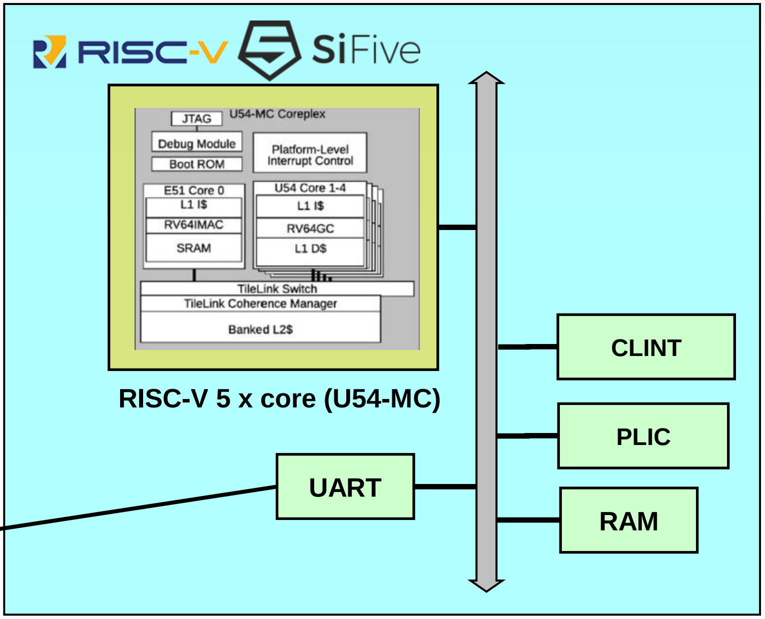
Agenda

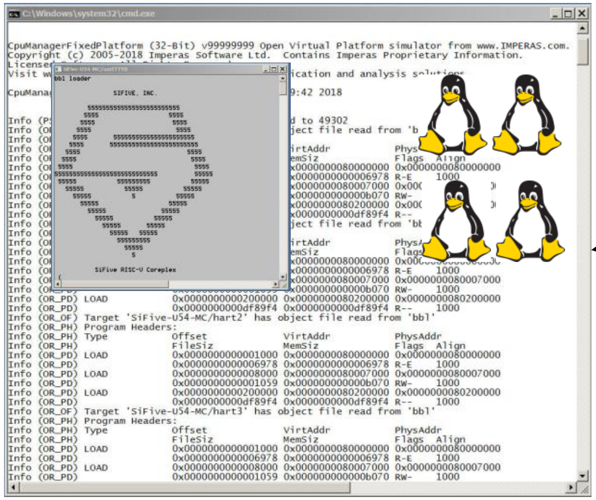
- Embedded Software Development Challenges
- Traditional SW Debug Environment using Hardware
- Modern SW Debug using Imperas Simulation
- Giving more visibility to SW Debug using UltraSoC Hardware
- Imperas/UltraSoC collaboration provides common solution

Simulating Hardware (Virtual Platforms) with Imperas

- Virtual Platforms built using processor, peripheral and platform models using Open Virtual Platforms (OVP) APIs
  - Models are open source
- Simulated unmodified production binaries
- Software does not know it is not on hardware
- Runs very fast, 100-2,000MIPS

Imperas U54-MC Virtual Platform



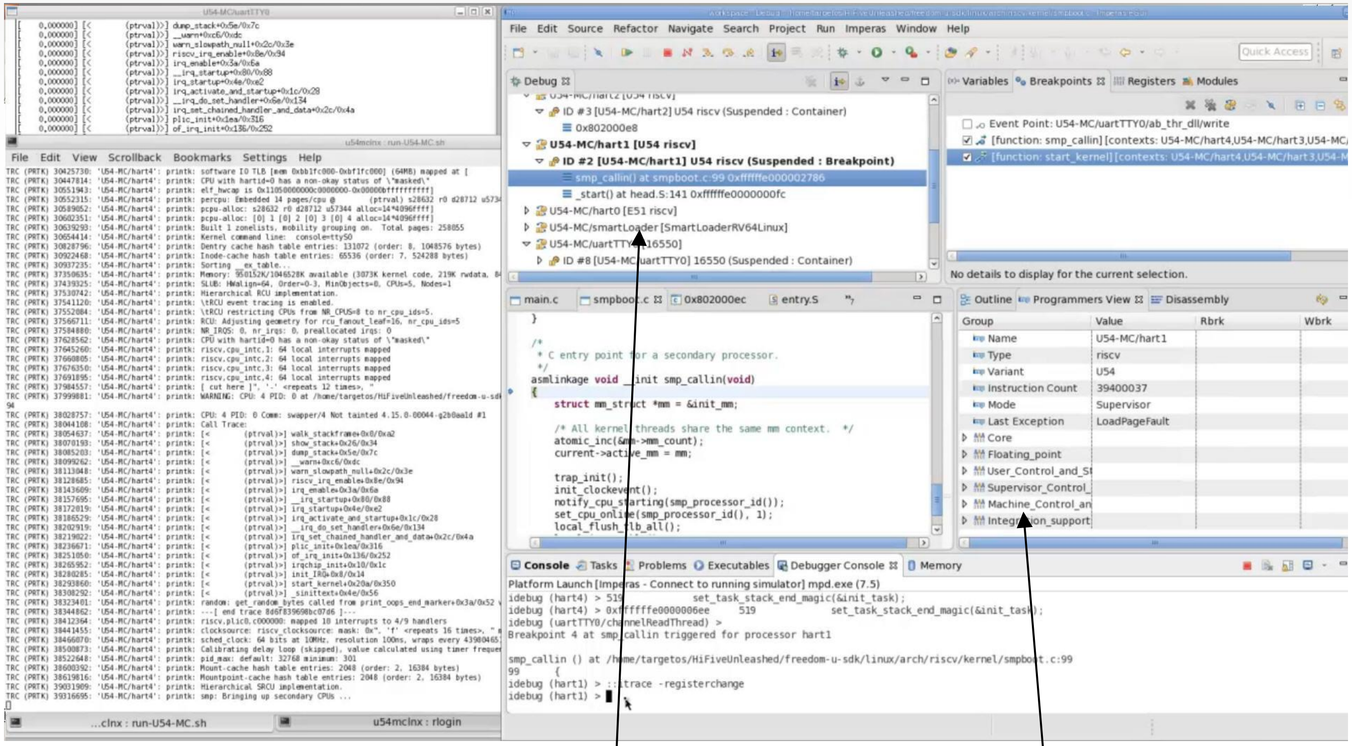


```
CpuManagerFixedPlatform (32-Bit) v99999999 Open Virtual Platform simulator from www.IMPERAS.com.
Copyright (c) 2005-2018 Imperas Software Ltd.  Contains Imperas Proprietary Information.
Info (OR_PD) LOAD              0x0000000000200000 0x0000000080200000 0x0000000080200000
Info (OR_PD)                   0x00000000000df89f4 0x0000000000df89f4 R--     1000
Info (OR_OF) Target 'SiFive-U54-MC/hart2' has object file read from 'bbl'
Info (OR_PH) Program Headers:
Info (OR_PH) Type              Offset             VirtAddr           PhysAddr
Info (OR_PH)                   FileSiz            MemSiz             Flags   Align
Info (OR_PD) LOAD              0x0000000000001000 0x0000000080000000 0x0000000080000000
Info (OR_PD)                   0x0000000000006978 0x0000000000006978 R-E     1000
Info (OR_PD) LOAD              0x0000000000008000 0x0000000080007000 0x0000000080007000
Info (OR_PD)                   0x0000000000001059 0x000000000000b070 RW-     1000
Info (OR_PD) LOAD              0x0000000000200000 0x0000000080200000 0x0000000080200000
Info (OR_PD)                   0x0000000000df89f4 0x0000000000df89f4 R--     1000
Info (OR_OF) Target 'SiFive-U54-MC/hart3' has object file read from 'bbl'
Info (OR_PH) Program Headers:
Info (OR_PH) Type              Offset             VirtAddr           PhysAddr
Info (OR_PH)                   FileSiz            MemSiz             Flags   Align
Info (OR_PD) LOAD              0x0000000000001000 0x0000000080000000 0x0000000080000000
Info (OR_PD)                   0x0000000000006978 0x0000000000006978 R-E     1000
Info (OR_PD) LOAD              0x0000000000008000 0x0000000080007000 0x0000000080007000
Info (OR_PD)                   0x0000000000001059 0x000000000000b070 RW-     1000
```

Under 10 seconds to get to booted Linux login prompt!

Imperas MPD
full platform debugger

- Platform aware, multiprocessor / multicore aware
- Driver-peripheral software-hardware co-debug
- Event-based debug, e.g. using assertions
- OS-aware debug, e.g. breakpoints on OS events


U54-MC/uartTTY0
u54mclnx : run-U54-MC.sh
File Edit View Scrollback Bookmarks Settings Help
File Edit Source Refactor Navigate Search Project Run Imperas Window Help
Quick Access
Debug
Variables Breakpoints Registers Modules
main.c smpboot.c 0x802000ec entry.S
Outline Programmers View Disassembly
Console Tasks Problems Executables Debugger Console Memory
...clnx : run-U54-MC.sh
u54mclnx : rlogin

```
[      0,000000] [<         (ptrval)>] dump_stack+0x5e/0x7c
[      0,000000] [<         (ptrval)>] __warn+0xc6/0xdc
[      0,000000] [<         (ptrval)>] warn_slowpath_null+0x2c/0x3e
[      0,000000] [<         (ptrval)>] riscv_irq_enable+0x8e/0x94
[      0,000000] [<         (ptrval)>] irq_enable+0x3a/0x6a
[      0,000000] [<         (ptrval)>] __irq_startup+0x80/0x88
[      0,000000] [<         (ptrval)>] irq_startup+0x4e/0xe2
[      0,000000] [<         (ptrval)>] irq_activate_and_startup+0x1c/0x28
[      0,000000] [<         (ptrval)>] __irq_do_set_handler+0x6e/0x134
[      0,000000] [<         (ptrval)>] irq_set_chained_handler_and_data+0x2c/0x4a
[      0,000000] [<         (ptrval)>] plic_init+0x1ea/0x316
[      0,000000] [<         (ptrval)>] of_irq_init+0x136/0x252
```

```
TRC (PRTK) 30425730: 'U54-MC/hart4': printk: software IO TLB [mem 0xbb1fc000-0xbf1fc000] (64MB) mapped at [
TRC (PRTK) 30447814: 'U54-MC/hart4': printk: CPU with hartid=0 has a non-okay status of \"masked\"
TRC (PRTK) 30551943: 'U54-MC/hart4': printk: elf_hwcap is 0x1105000000c0000000-0x00000bffffffffff]
TRC (PRTK) 30552315: 'U54-MC/hart4': printk: percpu: Embedded 14 pages/cpu @         (ptrval) s28632 r0 d28712 u5734
TRC (PRTK) 30589052: 'U54-MC/hart4': printk: pcpu-alloc: s28632 r0 d28712 u57344 alloc=14*4096ffff]
TRC (PRTK) 30602351: 'U54-MC/hart4': printk: pcpu-alloc: [0] 1 [0] 2 [0] 3 [0] 4 alloc=14*4096ffff]
TRC (PRTK) 30639293: 'U54-MC/hart4': printk: Built 1 zonelists, mobility grouping on.  Total pages: 258055
TRC (PRTK) 30654414: 'U54-MC/hart4': printk: Kernel command line:  console=ttyS0
TRC (PRTK) 30828796: 'U54-MC/hart4': printk: Dentry cache hash table entries: 131072 (order: 8, 1048576 bytes)
TRC (PRTK) 30922468: 'U54-MC/hart4': printk: Inode-cache hash table entries: 65536 (order: 7, 524288 bytes)
TRC (PRTK) 30937235: 'U54-MC/hart4': printk: Sorting __ex_table...
TRC (PRTK) 37350635: 'U54-MC/hart4': printk: Memory: 950152K/1046528K available (3073K kernel code, 219K rwdata, 84
TRC (PRTK) 37439325: 'U54-MC/hart4': printk: SLUB: HWalign=64, Order=0-3, MinObjects=0, CPUs=5, Nodes=1
TRC (PRTK) 37530742: 'U54-MC/hart4': printk: Hierarchical RCU implementation.
TRC (PRTK) 37541120: 'U54-MC/hart4': printk: \tRCU event tracing is enabled.
TRC (PRTK) 37552084: 'U54-MC/hart4': printk: \tRCU restricting CPUs from NR_CPUS=8 to nr_cpu_ids=5.
TRC (PRTK) 37566711: 'U54-MC/hart4': printk: RCU: Adjusting geometry for rcu_fanout_leaf=16, nr_cpu_ids=5
TRC (PRTK) 37584880: 'U54-MC/hart4': printk: NR_IRQS: 0, nr_irqs: 0, preallocated irqs: 0
TRC (PRTK) 37628562: 'U54-MC/hart4': printk: CPU with hartid=0 has a non-okay status of \"masked\"
TRC (PRTK) 37645260: 'U54-MC/hart4': printk: riscv,cpu_intc,1: 64 local interrupts mapped
TRC (PRTK) 37660805: 'U54-MC/hart4': printk: riscv,cpu_intc,2: 64 local interrupts mapped
TRC (PRTK) 37676350: 'U54-MC/hart4': printk: riscv,cpu_intc,3: 64 local interrupts mapped
TRC (PRTK) 37691895: 'U54-MC/hart4': printk: riscv,cpu_intc,4: 64 local interrupts mapped
TRC (PRTK) 37984557: 'U54-MC/hart4': printk: [ cut here ]", '-' <repeats 12 times>, "
TRC (PRTK) 37999881: 'U54-MC/hart4': printk: WARNING: CPU: 4 PID: 0 at /home/targetos/HiFiveUnleashed/freedom-u-sdk
94
TRC (PRTK) 38028757: 'U54-MC/hart4': printk: CPU: 4 PID: 0 Comm: swapper/4 Not tainted 4.15.0-00044-g2b0aald #1
TRC (PRTK) 38044108: 'U54-MC/hart4': printk: Call Trace:
TRC (PRTK) 38054637: 'U54-MC/hart4': printk: [<         (ptrval)>] walk_stackframe+0x0/0xa2
TRC (PRTK) 38070193: 'U54-MC/hart4': printk: [<         (ptrval)>] show_stack+0x26/0x34
TRC (PRTK) 38085203: 'U54-MC/hart4': printk: [<         (ptrval)>] dump_stack+0x5e/0x7c
TRC (PRTK) 38099262: 'U54-MC/hart4': printk: [<         (ptrval)>] __warn+0xc6/0xdc
TRC (PRTK) 38113048: 'U54-MC/hart4': printk: [<         (ptrval)>] warn_slowpath_null+0x2c/0x3e
TRC (PRTK) 38128685: 'U54-MC/hart4': printk: [<         (ptrval)>] riscv_irq_enable+0x8e/0x94
TRC (PRTK) 38143609: 'U54-MC/hart4': printk: [<         (ptrval)>] irq_enable+0x3a/0x6a
TRC (PRTK) 38157695: 'U54-MC/hart4': printk: [<         (ptrval)>] __irq_startup+0x80/0x88
TRC (PRTK) 38172019: 'U54-MC/hart4': printk: [<         (ptrval)>] irq_startup+0x4e/0xe2
TRC (PRTK) 38186529: 'U54-MC/hart4': printk: [<         (ptrval)>] irq_activate_and_startup+0x1c/0x28
TRC (PRTK) 38202919: 'U54-MC/hart4': printk: [<         (ptrval)>] __irq_do_set_handler+0x6e/0x134
TRC (PRTK) 38219022: 'U54-MC/hart4': printk: [<         (ptrval)>] irq_set_chained_handler_and_data+0x2c/0x4a
TRC (PRTK) 38236671: 'U54-MC/hart4': printk: [<         (ptrval)>] plic_init+0x1ea/0x316
TRC (PRTK) 38251050: 'U54-MC/hart4': printk: [<         (ptrval)>] of_irq_init+0x136/0x252
TRC (PRTK) 38265952: 'U54-MC/hart4': printk: [<         (ptrval)>] irqchip_init+0x10/0x1c
TRC (PRTK) 38280285: 'U54-MC/hart4': printk: [<         (ptrval)>] init_IRQ+0x8/0x14
TRC (PRTK) 38293860: 'U54-MC/hart4': printk: [<         (ptrval)>] start_kernel+0x20a/0x350
TRC (PRTK) 38308292: 'U54-MC/hart4': printk: [<         (ptrval)>] _sinittext+0x4e/0x56
TRC (PRTK) 38323401: 'U54-MC/hart4': printk: random: get_random_bytes called from print_oops_end_marker+0x3a/0x52 v
TRC (PRTK) 38344862: 'U54-MC/hart4': printk: ---[ end trace 8d6f839698bc07d6 ]---
TRC (PRTK) 38412364: 'U54-MC/hart4': printk: riscv,plic0,c000000: mapped 10 interrupts to 4/9 handlers
TRC (PRTK) 38441455: 'U54-MC/hart4': printk: clocksource: riscv_clocksource: mask: 0x", 'f' <repeats 16 times>, " m
TRC (PRTK) 38466070: 'U54-MC/hart4': printk: sched_clock: 64 bits at 10MHz, resolution 100ns, wraps every 43980465
TRC (PRTK) 38500873: 'U54-MC/hart4': printk: Calibrating delay loop (skipped), value calculated using timer frequen
TRC (PRTK) 38522648: 'U54-MC/hart4': printk: pid_max: default: 32768 minimum: 301
TRC (PRTK) 38600392: 'U54-MC/hart4': printk: Mount-cache hash table entries: 2048 (order: 2, 16384 bytes)
TRC (PRTK) 38619816: 'U54-MC/hart4': printk: Mountpoint-cache hash table entries: 2048 (order: 2, 16384 bytes)
TRC (PRTK) 39031909: 'U54-MC/hart4': printk: Hierarchical SRCU implementation.
TRC (PRTK) 39316695: 'U54-MC/hart4': printk: smp: Bringing up secondary CPUs ...
```

U54-MC/hart2 [U54 riscv]
- ID #3 [U54-MC/hart2] U54 riscv (Suspended : Container)
  - 0x802000e8

U54-MC/hart1 [U54 riscv]
- **ID #2 [U54-MC/hart1] U54 riscv (Suspended : Breakpoint)**
  - smp_callin() at smpboot.c:99 0xffffffe000002786
  - _start() at head.S:141 0xffffffe0000000fc

U54-MC/hart0 [E51 riscv]

U54-MC/smartLoader [SmartLoaderRV64Linux]

U54-MC/uartTTY0 [16550]
- ID #8 [U54-MC/uartTTY0] 16550 (Suspended : Container)

☐ Event Point: U54-MC/uartTTY0/ab_thr_dll/write
☑ [function: smp_callin] [contexts: U54-MC/hart4,U54-MC/hart3,U54-MC/
☑ [function: start_kernel] [contexts: U54-MC/hart4,U54-MC/hart3,U54-M

No details to display for the current selection.

```
}

/*
 * C entry point for a secondary processor.
 */
asmlinkage void __init smp_callin(void)
{
	struct mm_struct *mm = &init_mm;

	/* All kernel threads share the same mm context.  */
	atomic_inc(&mm->mm_count);
	current->active_mm = mm;

	trap_init();
	init_clockevent();
	notify_cpu_starting(smp_processor_id());
	set_cpu_online(smp_processor_id(), 1);
	local_flush_tlb_all();
```

Group	Value	Rbrk	Wbrk
Name	U54-MC/hart1		
Type	riscv		
Variant	U54		
Instruction Count	39400037		
Mode	Supervisor		
Last Exception	LoadPageFault		
▷ Core			
▷ Floating_point			
▷ User_Control_and_St			
▷ Supervisor_Control_			
▷ Machine_Control_an			
▷ Integration_support			

```
Platform Launch [Imperas - Connect to running simulator] mpd.exe (7.5)
idebug (hart4) > 519            set_task_stack_end_magic(&init_task);
idebug (hart4) > 0xffffffe0000006ee     519             set_task_stack_end_magic(&init_task);
idebug (uartTTY0/channelReadThread) >
Breakpoint 4 at smp_callin triggered for processor hart1

smp_callin () at /home/targetos/HiFiveUnleashed/freedom-u-sdk/linux/arch/riscv/kernel/smpboot.c:99
99      {
idebug (hart1) > ::itrace -registerchange
idebug (hart1) > █
```

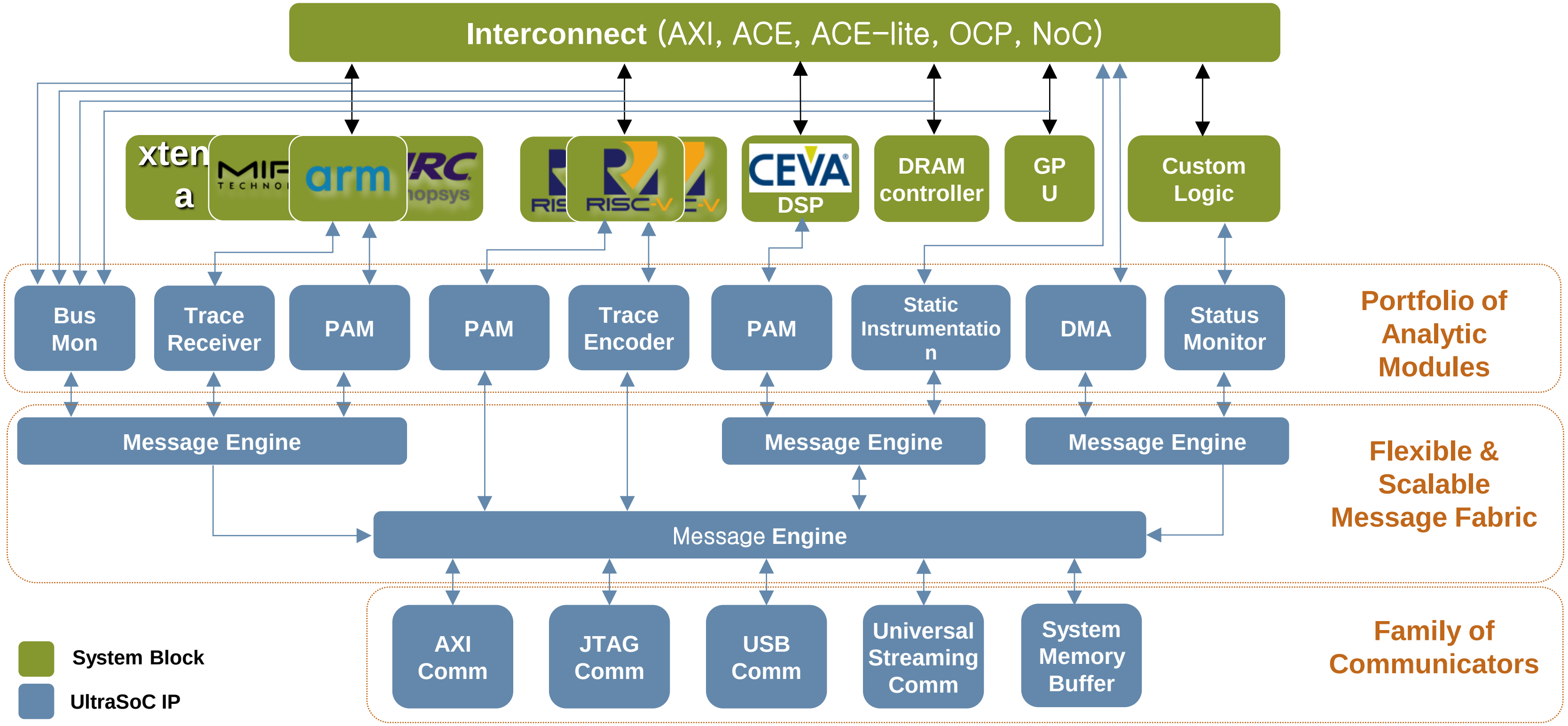
Select CPU or peripheral in target window and see source, programmers registers, variables, …

Complete visibility in platform…

Agenda

- Embedded Software Development Challenges
- Traditional SW Debug Environment using Hardware
- Modern SW Debug using Imperas Simulation
- Giving more visibility to SW Debug using UltraSoC Hardware
- Imperas/UltraSoC collaboration provides common solution

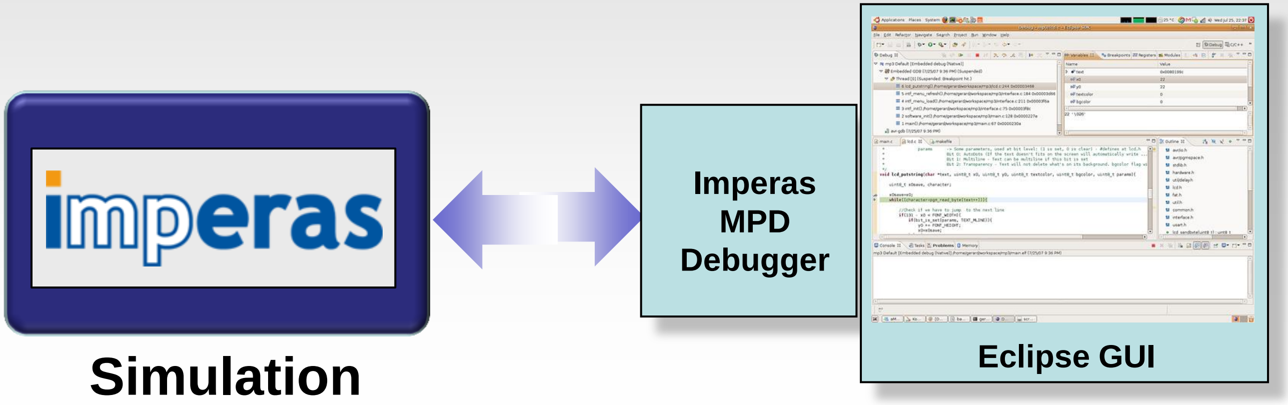
Advanced debug/monitoring for the whole SoC

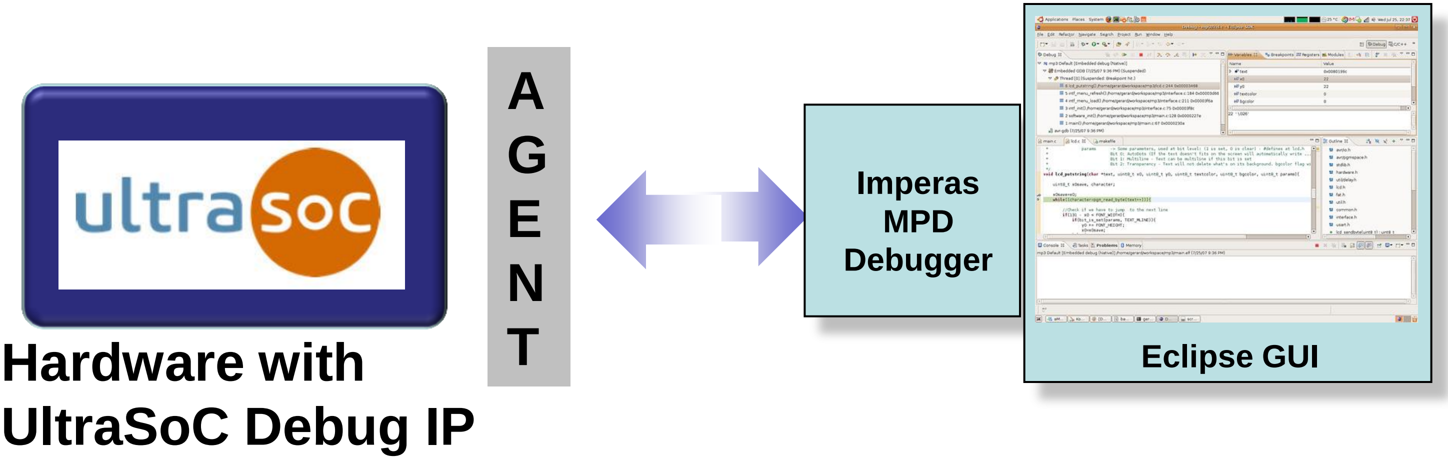


Agenda

- Embedded Software Development Challenges
- Traditional SW Debug Environment using Hardware
- Modern SW Debug using Imperas Simulation
- Giving more visibility to SW Debug using UltraSoC Hardware
- Imperas/UltraSoC collaboration provides common solution

Collaboration





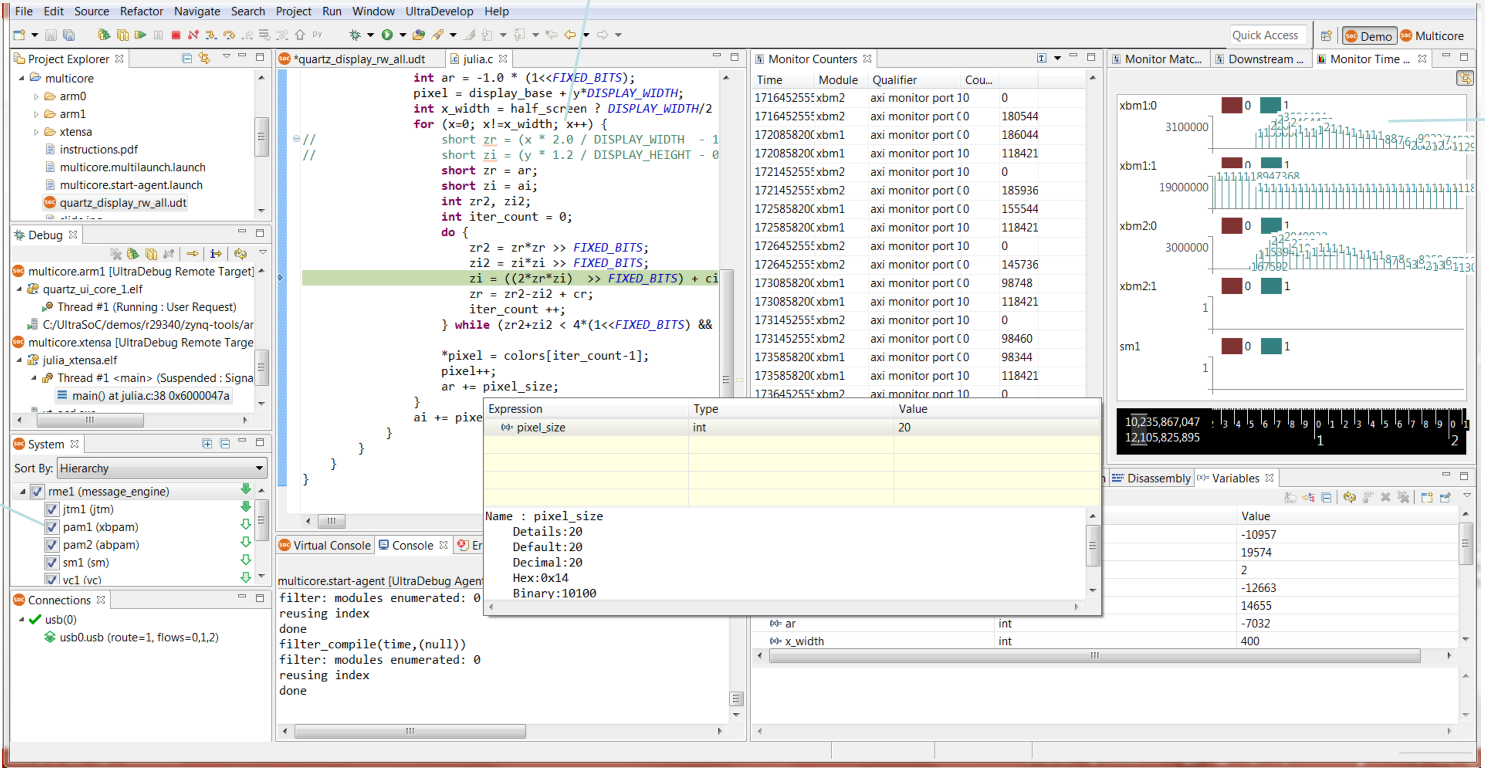
- Common Software Development Environment

Collaboration allows use from concept to production

Visibility of software

Bus activity

Control configuration



- multicore
  - arm0
  - arm1
  - xtensa
  - instructions.pdf
  - multicore.multilaunch.launch
  - multicore.start-agent.launch
  - quartz_display_rw_all.udt

- multicore.arm1 [UltraDebug Remote Target]
  - quartz_ui_core_1.elf
    - Thread #1 (Running : User Request)
  - C:/UltraSoC/demos/r29340/zynq-tools/ar
- multicore.xtensa [UltraDebug Remote Targe
  - julia_xtensa.elf
    - Thread #1 <main> (Suspended : Signa
      - main() at julia.c:38 0x6000047a

Sort By: Hierarchy

- ☑ rme1 (message_engine)
  - ☑ jtm1 (jtm)
  - ☑ pam1 (xbpam)
  - ☑ pam2 (abpam)
  - ☑ sm1 (sm)
  - ☑ vc1 (vc)

- ✓ usb(0)
  - usb0.usb (route=1, flows=0,1,2)

```
                int ar = -1.0 * (1<<FIXED_BITS);
                pixel = display_base + y*DISPLAY_WIDTH;
                int x_width = half_screen ? DISPLAY_WIDTH/2
                for (x=0; x!=x_width; x++) {
//                  short zr = (x * 2.0 / DISPLAY_WIDTH  - 1
//                  short zi = (y * 1.2 / DISPLAY_HEIGHT - 0
                    short zr = ar;
                    short zi = ai;
                    int zr2, zi2;
                    int iter_count = 0;
                    do {
                        zr2 = zr*zr >> FIXED_BITS;
                        zi2 = zi*zi >> FIXED_BITS;
                        zi = ((2*zr*zi)  >> FIXED_BITS) + ci
                        zr = zr2-zi2 + cr;
                        iter_count ++;
                    } while (zr2+zi2 < 4*(1<<FIXED_BITS) &&

                    *pixel = colors[iter_count-1];
                    pixel++;
                    ar += pixel_size;
                }
                ai += pixe
            }
        }
    }
}
```

Time	Module	Qualifier	Cou...	
1716452555	xbm2	axi monitor port 1	0	0
1716452555	xbm2	axi monitor port (	0	180544
172085820(	xbm1	axi monitor port (	0	186044
172085820(	xbm1	axi monitor port 1	0	118421
1721452555	xbm2	axi monitor port 1	0	0
1721452555	xbm2	axi monitor port (	0	185936
172585820(	xbm1	axi monitor port (	0	155544
172585820(	xbm1	axi monitor port 1	0	118421
1726452555	xbm2	axi monitor port 1	0	0
1726452555	xbm2	axi monitor port (	0	145736
173085820(	xbm1	axi monitor port (	0	98748
173085820(	xbm1	axi monitor port 1	0	118421
1731452555	xbm2	axi monitor port 1	0	0
1731452555	xbm2	axi monitor port (	0	98460
173585820(	xbm1	axi monitor port (	0	98344
173585820(	xbm1	axi monitor port 1	0	118421
1736452555	xbm2	axi monitor port 1	0	0

Expression	Type	Value
pixel_size	int	20

```
Name : pixel_size
    Details:20
    Default:20
    Decimal:20
    Hex:0x14
    Binary:10100
```

```
multicore.start-agent [UltraDebug Agent
filter: modules enumerated: 0
reusing index
done
filter_compile(time,(null))
filter: modules enumerated: 0
reusing index
done
```

		Value
		-10957
		19574
		2
		-12663
		14655
ar	int	-7032
x_width	int	400

- Views to control and debug and observe throughout the design process

Summary

- Imperas and UltraSoC collaborating
  - Developing common software development environment
  - Same for hardware based and simulation based teams

- Start with simulation on virtual platforms
- Use with RTL as design progresses
- Use prototypes when available
- Use with silicon pre- and post- production