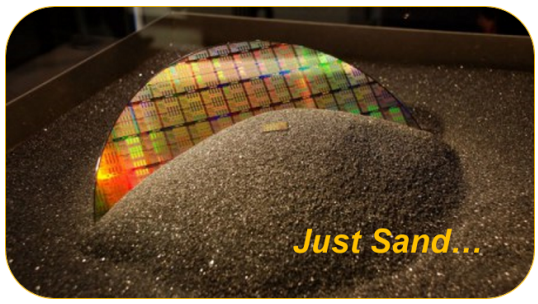
Revolutionizing Embedded Software Development

Imperas Newsletter May 2015

"Silicon without software is just sand."

Welcome to the Imperas Newsletter!
Updating you on what's new in our embedded software revolution.



CEO View: Simon Davidmann

As we move into the middle of 2015, it is timely to address three key realities of our businesses.

Here are a few observations on developing embedded software:
As software complexity is increasing exponentially, companies need to adopt better ways to address problems, as eventually the existing methods will no longer be sufficient. (VDC researchers found that the size of embedded code bases is growing at roughly twice the speed of the embedded developer community.)

One serious failure changes everything. Think of car braking systems, avionics communications, or steering electronics. Think of the challenges we increasingly face in the security arena, which includes all levels of software as well as the underlying hardware.

There are lessons to be learned from SoC design and verification:a structured approach/methodology provides predictable execution and measurable reduction of risk.
So, the embedded software development domain needs to adopt a more formalized approach. One key technology and methodology for embedded software and systems design is the use of virtual platforms, with high level software simulation.

At Imperas, we have always led the way with virtual prototyping technology, one of the key solutions for embedded software development. We look forward to working with you on all the exciting possibilities ahead!

Recore Systems Selects Imperas for Virtual Platform Software Development Tools

Imperas extendable platform kit accelerates development for Recore

many-core hardware and software program.

Recore is building a new many-core hardware platform for applications such as embedded vision, and selected Imperas for virtual platform-based software development. The new Recore FlexaWare platform is a many-core embedded system with three closely connected components: many-core hardware, a runtime (many-core) OS, and a software development environment.

As the platform was built from the ground up, it was imperative to test important design concepts immediately in a simulation environment, to confirm that they function as expected. Since time to market was crucial, Recore Systems searched for a simulation framework that could support design space exploration as well as software development and test. Recore selected Imperas because of the nature of the components already on offer, and started quickly by using an Imperas Extendable Platform Kit™ (EPK™).
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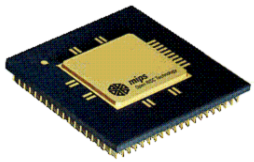

Fast Processor Models of MIPS Warrior Cores Released by Imperas and Open Virtual Platforms

Imperas Virtual Platform Products Provide Interface to Imagination Codescape Debugger.

Using MIPS processors in your development? Imperas has released Open Virtual Platforms™ (OVP™) Fast Processor Models for the MIPS Warrior P-class and M-class CPU IP cores from Imagination Technologies. Example virtual platforms are also provided, as well as support for the cores in the Imperas M*SDK™ advanced software development tools. In addition, the Imperas M*SDK and M*DEV™ products support the use of the Imagination Codescape Debugger for embedded software debug and development.

The processor core models and example platforms are available from the Open Virtual Platforms website. The models of the P5600 and M51xx processor cores, as well as models of other MIPS processors, work with the Imperas and OVP simulators, including the Imperas QuantumLeap™ parallel simulation accelerator, and have shown exceptionally fast performance of hundreds of millions of instructions per second.
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Magillem Partnering with Imperas: Enabling IoT Using Virtual Platforms

Explosion in IoT (Internet of Things)! Sensor-laden intelligent devices are expanding our world, and changing the way we design systems. IoT fuels growth of products and services in automotive, medical, commerce and more. Magillem, provider of front-end design xml solutions and tools to reduce the global cost of complex designs, has partnered with Imperas to leverage Imperas models in its X-Spec solution.

Increased software functionality, coupled with multiple IoT nodes concurrency, has increased the complexity and scale of embedded software in typical development projects. The software component of these projects already represents their largest cost center, and the increase in concurrency sends design productivity barriers spiraling out of control. Virtual platform techniques are more than ever the best way to accelerate embedded software development and provide early validation of systems.
Read more...

Imagination Blog: New MIPS Models from Imperas

Larry Lapides, VP of Sales at Imperas, explains about the collaboration between Imperas and Imagination as well as the wide range of solutions available for MIPS CPUs.

A lot has been happening in OVP (Open Virtual Platforms) for the MIPS world! You are probably aware that Imperas designs simulation tools and technologies for MIPS CPUs from Imagination Technologies. Now, a complete modeling and development platform is available from Imperas for the latest MIPS P-Class and M-Class Warrior CPU IP cores. What does this include? Models of the P5600 and M51xx processor IP cores, as well as models of other MIPS processors. EPKs of the MIPS-based platforms. These models and example platforms are available now, from the Open Virtual Platforms website.

The complete development platform includes these models, supported in the Imperas M*SDK™ advanced software development tools, and working with the Imperas and OVP simulators, including the QuantumLeap parallel simulation accelerator. In addition, the Imperas M*SDK and M*DEV™ products support the use of the Imagination Codescape Debugger for embedded software debug.

Want proof? Kyma Systems has already used Imperas tools and models to port the KVM hypervisor to MIPS. And, Imperas is the proud provider of the technology behind the IASim product from Imagination, the instruction-accurate simulator for MIPS cores.
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Nikkei Electronics Article: Imperas and FPGAs

For our Japanese readership.

Sugoi! Read the Nikkei Electronics commentary on Imperas and FPGAs. It features advanced Altera integrated-core FPGAs, and how Imperas virtual platforms for these FPGAs allow developers to execute operating system and software stacks, rapidly and easily.
Read more....

Embedded COMPUTING DESIGN

Embedded Computing Design on Imperas and MIPS

Rich Nass commentary on Imperas release of OVP Fast Processor Models and virtual platforms for Imagination Technologies MIPS Warrior IP cores.

The MIPS platform got a big boost with a recent series of announcements. First, Imperas is releasing the Open Virtual Platforms (OVP) Fast Processor Models for the MIPS Warrior P-class and M-class CPU IP cores from Imagination Technologies. Example virtual platforms are also being released, as well as support for the cores in the Imperas M*SDK advanced software development tools. Also, the Imperas M*SDK and M*DEV products support the Imagination Codescape Debugger for embedded software debug and development.

The P5600 and M51xx processor cores, as well as models of other MIPS processors, work with the Imperas and OVP simulators, including the QuantumLeap parallel simulation accelerator. All OVP processor models are instruction accurate, and very fast, focused on enabling embedded software developers to have a development environment available early to accelerate the entire product development cycle. Virtual platforms using these processor models can be created with the OVP peripheral and platform models, or the processor models can be integrated into SystemC/TLM-2.0 based virtual platforms using the native TLM-2.0 interface available with all OVP processor models.
Read more...

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prpl for the People

Imperas a founding member of prpl Security PEG.

The prpl Foundation, an open-source non-profit foundation focused on enabling next-generation datacenter-to-device portable software and virtualized architectures, announced its Security PEG (prpl Engineering Group) in March. Imperas Software is a proud founding member of the Security PEG, dedicated to defining an open security framework for deploying secured and authenticated virtualized services in the IoT and related emerging markets.

The new Security PEG will define a security roadmap to get from today's software-virtualized solutions to full hardware supported virtualization, enabling multi-domain security across processors (CPUs, GPUs, NPUs), heterogeneous SoCs and systems built on these technologies including connected devices, routers and hubs. In addition, the Security PEG will define necessary open APIs (application programming interfaces) for various levels of the security stack.
Read more.....

Brian Bailey Blogs About His EDA Startups Panel

Are there problems ahead For EDA? A drought of new startups and lengthy exit strategies don't bode well for the industry.

Brian Bailey of Semiconductor Engineering sat down with Simon Davidmann, chief executive officer for Imperas; Bill Neifert, chief technology officer at Carbon Design Systems; Randy Smith, vice president of marketing for Sonics; and Michel Courtoy, vice president of marketing and business development for Kilopass Technology, to discuss the health of EDA.
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Imperas Talks About Parallel Simulation Acceleration

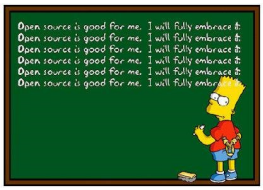
QuantumLeap paper presented at the Embedded World Conference in Nuremberg, Germany.

The embedded world Exhibition and Conference is the world's largest platform for embedded-system technologies and the knowledge tank of one of the most innovative sectors, featuring "the Internet of Things." Larry Lapides, Imperas Vice President of Sales, delivered a paper on QuantumLeap and multi-core software development, debug and test, emphasizing new parallelized virtual platform acceleration technology. QuantumLeap is a parallel simulation performance accelerator that leverages a new synchronization algorithm to provide the fastest virtual platform software execution speed available. The execution performance of this new technology has been measured on average at 15 times faster than the nearest commercial solution using standard benchmarks.

Many current System-on-Chip (SoC) hardware platforms, for example mobile and server devices, incorporate multi-core embedded processors coupled with hardware accelerators, all executing in parallel. Yet, the performance of existing, single-threaded virtual platform simulators did not adequately scale for these SoCs. Now, QuantumLeap eliminates this barrier by allocating the simulated cores across all processors in a host machine. With efficient synchronization of these cores, QuantumLeap delivers near-linear scaling of the simulation across the multiple host processors. Furthermore, QuantumLeap provides a transparent use model, with no change required to the software-under-test, the virtual platform models or the development environment, while ensuring fully deterministic simulation execution.
Read more.....

OVPsim Release News

OVP: Fast Simulation, Free open source models, Public APIs: Open Virtual Platforms.



The Open Virtual Platforms™ (OVP™) portal is one of the most exciting open source software developments in the embedded software world since GNU created GDB.

- For embedded software developers, virtual platforms will be increasingly important, especially for multi-core designs. The resources on this portal can significantly accelerate your development and test..

- Explore what is new at OVPworld!

The current OVPsim release is 20150205.0 (February 2015)

- Please check the release notes on OVPworld.org for more details.
- The next release of OVPsim is expected to be available in mid-May.

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