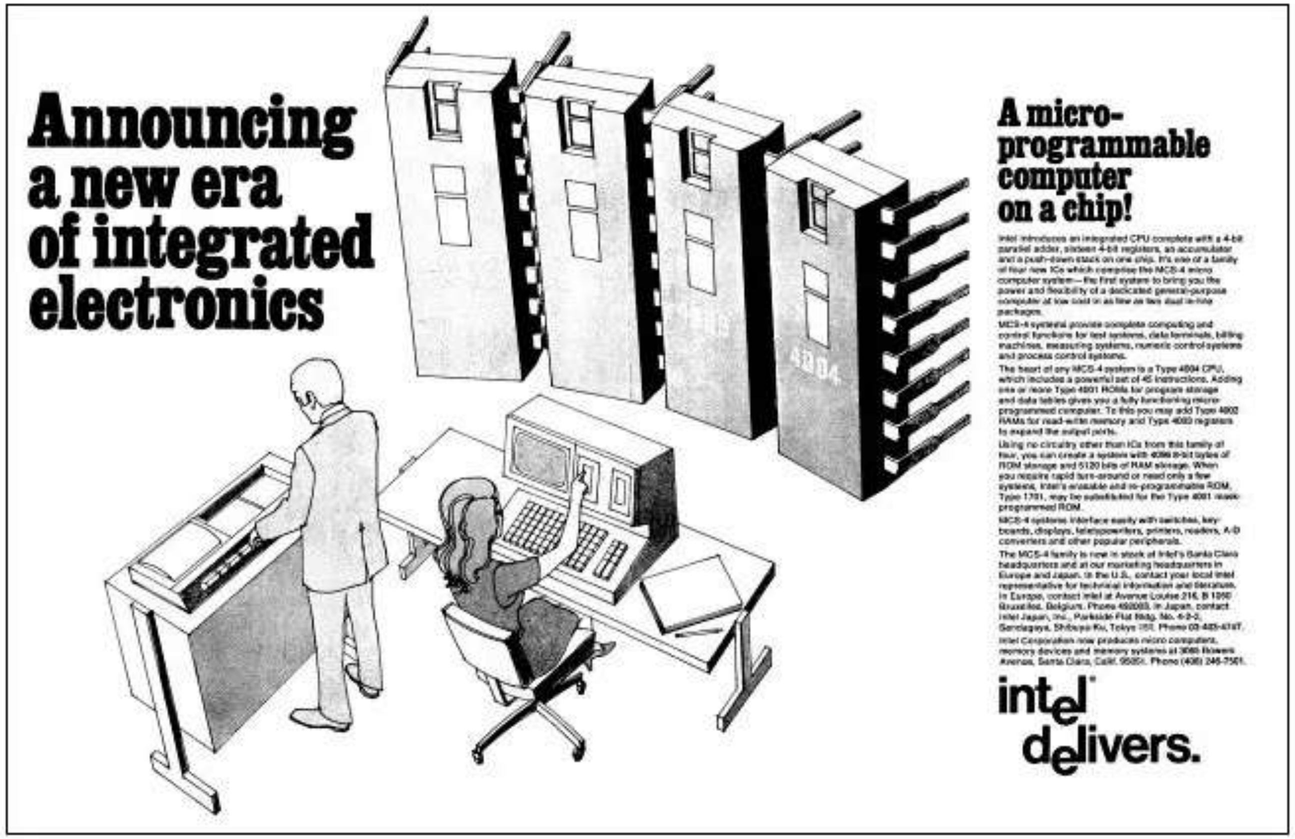
imperas

Is hardware/software co-design now a reality for applications with RISC-V?

RISC-V® Summit

Kevin McDermott, 8th December 2021

Microprocessor at 50 in 2021



Announcing a new era of integrated electronics

A micro-programmable computer on a chip!

Intel introduces an integrated CPU complete with a 4-bit parallel adder, sixteen 4-bit registers, an accumulator and a push-down stack on one chip. It's one of a family of four new ICs which comprise the MCS-4 micro computer system—the first system to bring you the power and flexibility of a dedicated general-purpose computer at low cost in as few as two dual in-line packages.

MCS-4 systems provide complete computing and control functions for test systems, data terminals, billing machines, measuring systems, numeric control systems and process control systems.

The heart of any MCS-4 system is a Type 4004 CPU, which includes a powerful set of 45 instructions. Adding one or more Type 4001 ROMs for program storage and data tables gives you a fully functioning micro-programmed computer. To this you may add Type 4002 RAMs for read-write memory and Type 4003 registers to expand the output ports.

Using no circuitry other than ICs from this family of four, you can create a system with 4096 8-bit bytes of ROM storage and 5120 bits of RAM storage. When you require rapid turn-around or need only a few systems, Intel's erasable and re-programmable ROM, Type 1701, may be substituted for the Type 4001 mask-programmed ROM.

MCS-4 systems interface easily with switches, keyboards, displays, teletypewriters, printers, readers, A-D converters and other popular peripherals.

The MCS-4 family is now in stock at Intel's Santa Clara headquarters and at our marketing headquarters in Europe and Japan. In the U.S., contact your local Intel representative for technical information and literature. In Europe, contact Intel at Avenue Louise 216, B 1050 Brussels, Belgium. Phone 492003. In Japan, contact Intel Japan, Inc., Parkside Flat Bldg. No. 4-2-2, Sendagaya, Shibuya-Ku, Tokyo 151. Phone 03-403-4747.

Intel Corporation now produces micro computers, memory devices and memory systems at 3065 Bowers Avenue, Santa Clara, Calif. 95051. Phone (408) 246-7501.

intel delivers.

The original November 15, 1971 ad for the Intel 4004. Intel

Microprocessor timeline (the first 50 years)

- Computer on a chip
- The RISC vs CISC wars
  - Can complexity help simplify the problem
- Desktop and embedded
  - Complexity and quality, embedded reliability for critical systems
- Supercomputer (Academic) -> Datacenter (Commercial)
  - Lots of compute resources, some cost/size/location implications
- Standard devices vs Application Specific Integrated Circuits (ASIC’s)
  - Design for the mass market or optimize systems performance at the chip level
- Multicore & SoC (System on Chip)
  - Heterogeneous, just the right features in just the right configuration
  - 10’s, 100’s, 1,000’s of cores…….

And do not forget about the software…..

- Programming languages
- Development tools
- Operating Systems and RTOS (Real-Time Operating System)
- Application software
- Internet
- Apps
- Games

Imperas

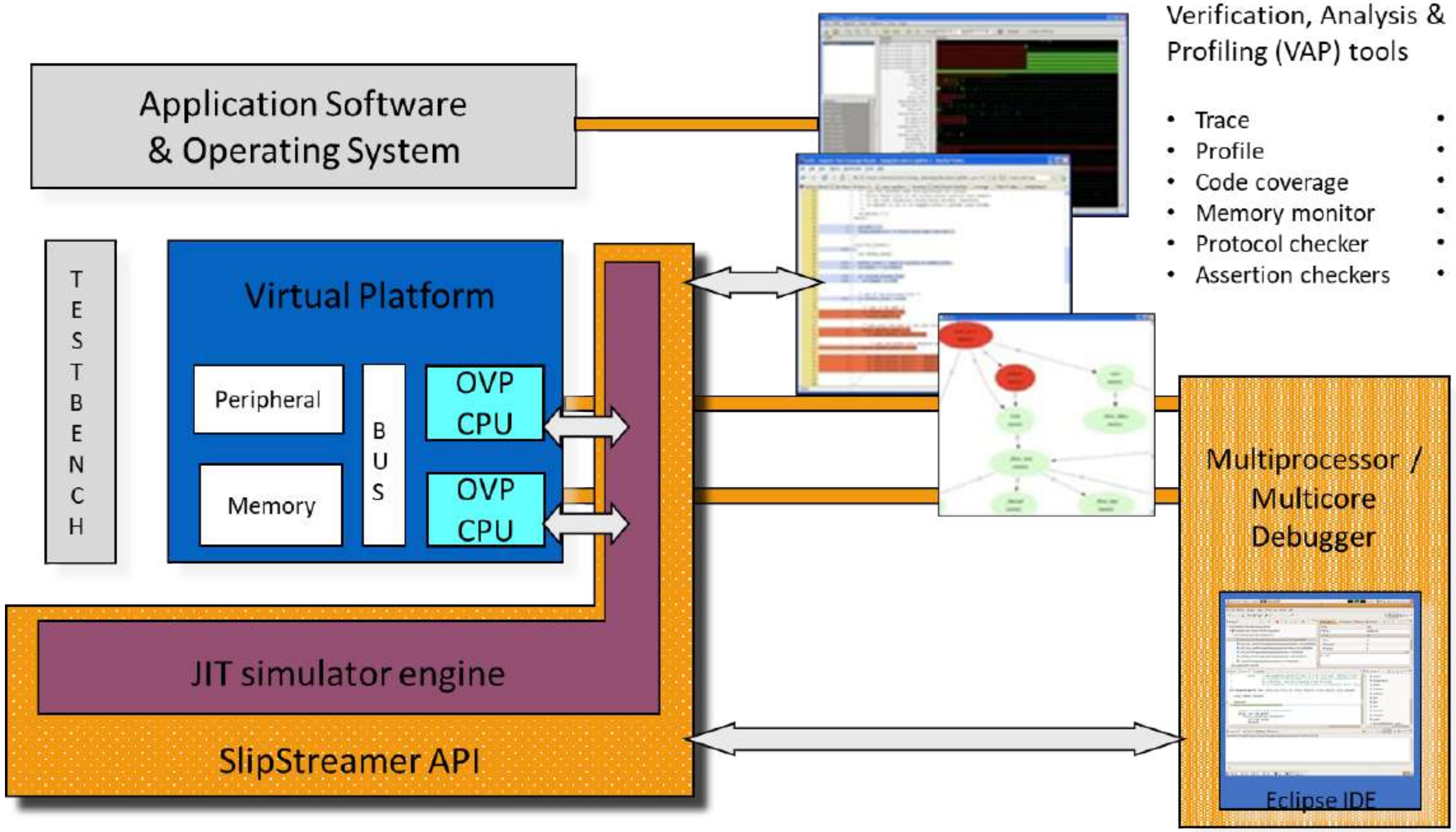
- “nobody designs a chip without simulation”,

  at Imperas we believe that:

“nobody should develop embedded software without simulation”

- Imperas develops simulators, tools, debuggers, modeling technology, and models to help embedded systems developers and SoC designers get their systems running… and their hardware verified
- 12+ years, self funded, profitable, UK based, team with much EDA (simulators, verification), processors, and embedded experience
- www.imperas.com   www.OVPworld.org

Simulation solutions for SW developers

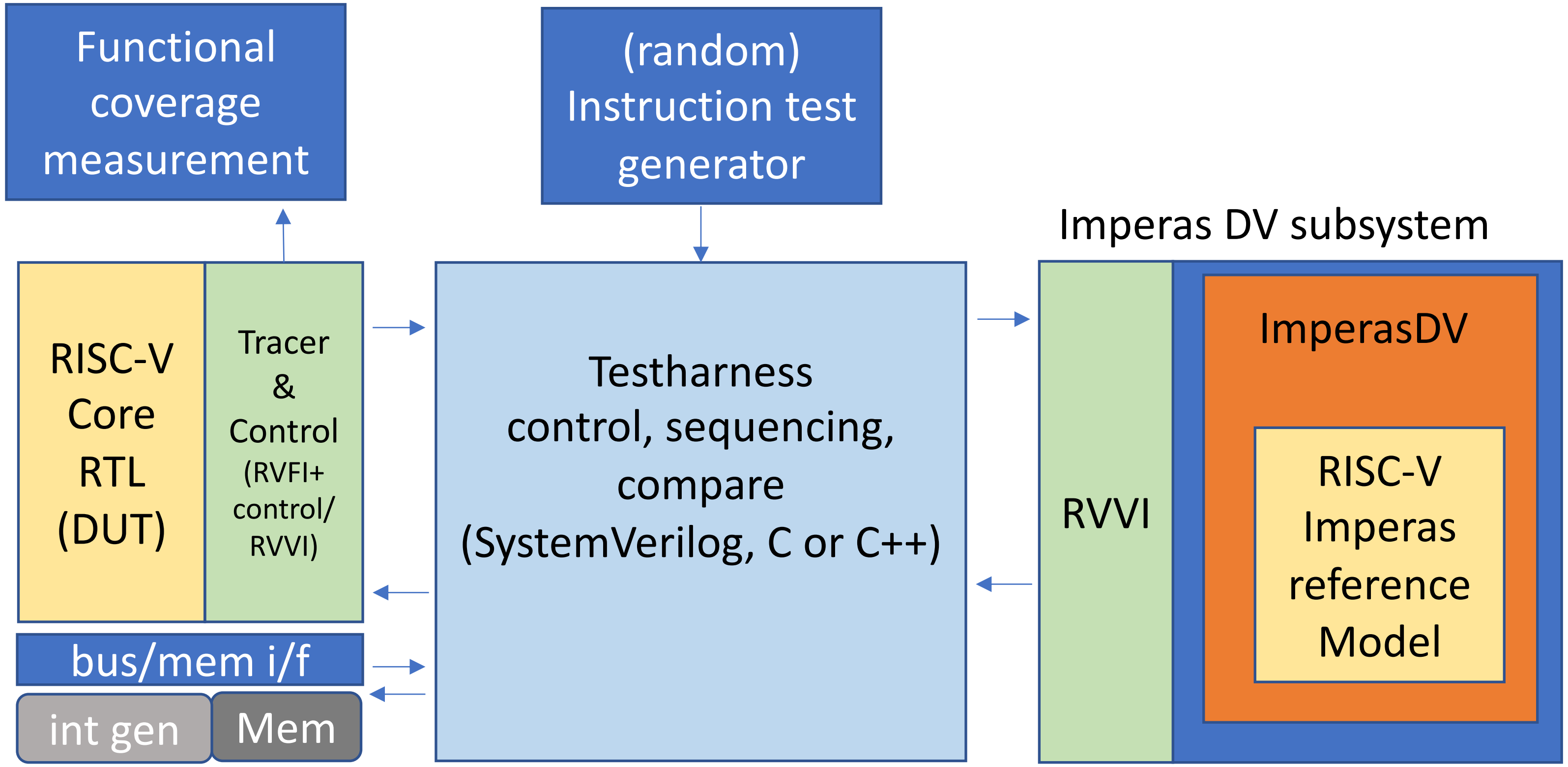


Verification, Analysis & Profiling (VAP) tools

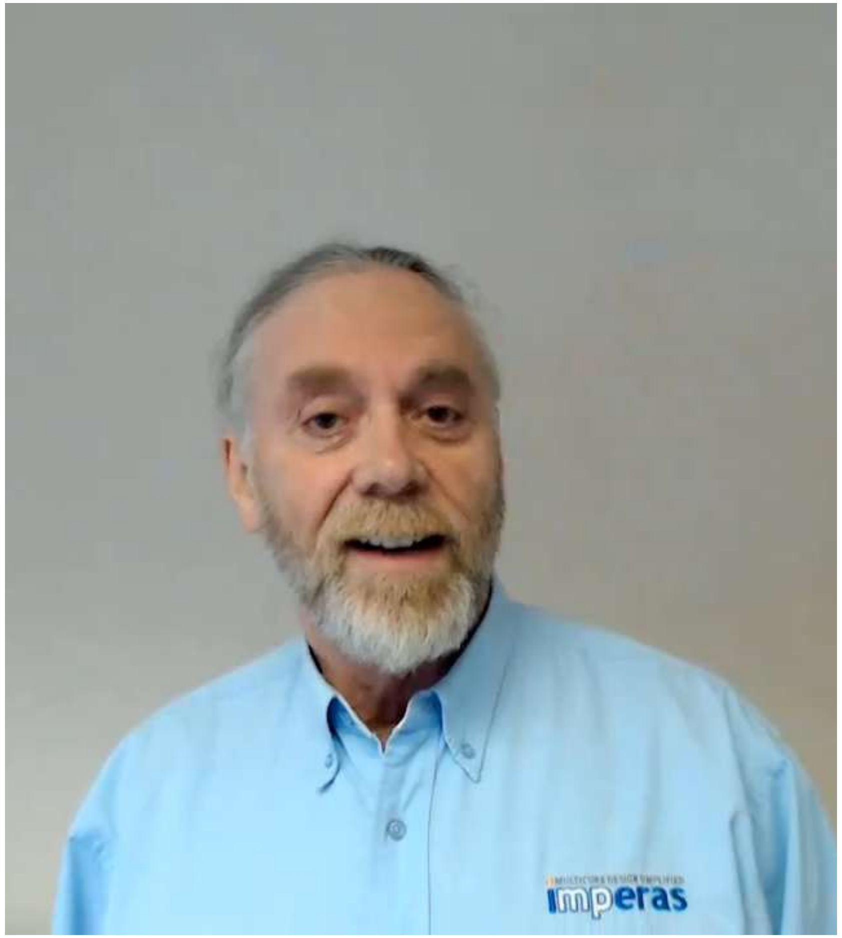
- Trace
- Profile
- Code coverage
- Memory monitor
- Protocol checker
- Assertion checkers
- OS task tracing
- OS scheduler analysis
- Fault injection
- Function tracing
- Variable tracing
- ...

- World class multicore simulator and full system emulator
- Library of advanced Verification, Analysis, Profiling tools
- Eclipse based Multiprocessor / Multicore debugger

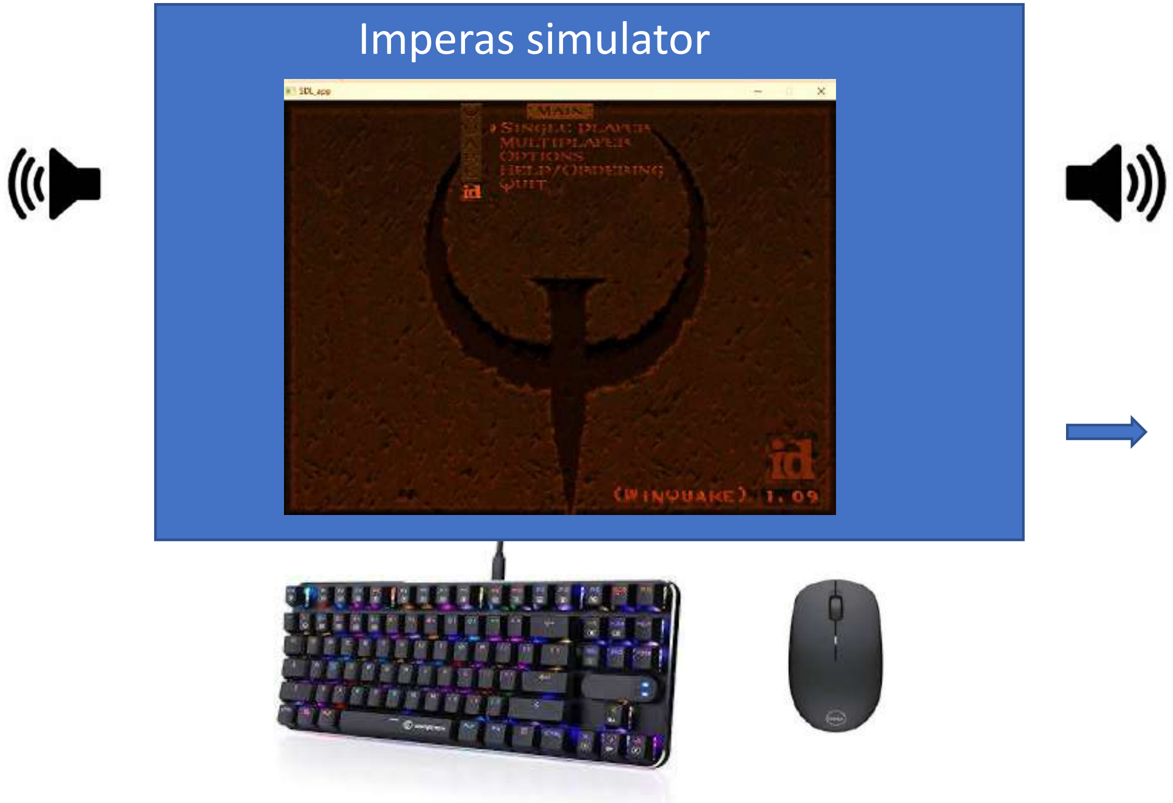
ImperasDV for RISC-V CPU Verification

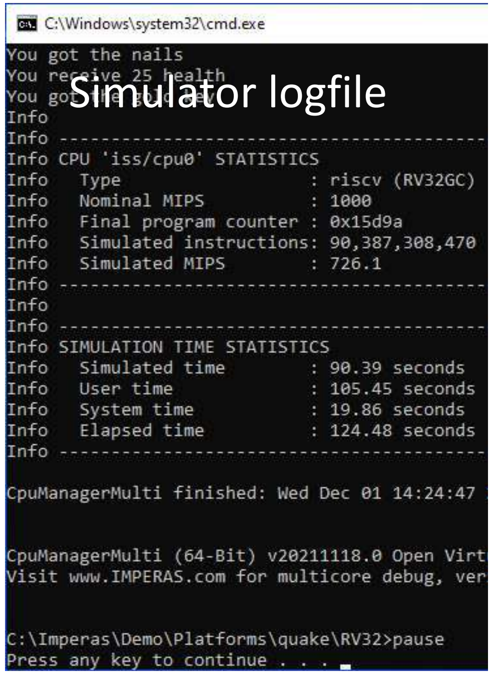

Functional coverage measurement
(random) Instruction test generator
Imperas DV subsystem
RISC-V Core RTL (DUT)
Tracer & Control (RVFI+ control/ RVVI)
Testharness control, sequencing, compare (SystemVerilog, C or C++)
RVVI
ImperasDV
RISC-V Imperas reference Model
bus/mem i/f
int gen
Mem

- New solution to make it easy to verify RISC-V processor
- Works with SystemVerilog or C/C++ and Verilator
- sync-lock-step-compare and async-lock-step-compare



Id Games QUAKE – on RISC-V





Simulator logfile

```
C:\Windows\system32\cmd.exe
You got the nails
You receive 25 health
You got the gold key
Info
Info ----------------------------------------
Info CPU 'iss/cpu0' STATISTICS
Info   Type                    : riscv (RV32GC)
Info   Nominal MIPS            : 1000
Info   Final program counter : 0x15d9a
Info   Simulated instructions: 90,387,308,470
Info   Simulated MIPS          : 726.1
Info ----------------------------------------
Info
Info ----------------------------------------
Info SIMULATION TIME STATISTICS
Info   Simulated time          : 90.39 seconds
Info   User time               : 105.45 seconds
Info   System time             : 19.86 seconds
Info   Elapsed time            : 124.48 seconds
Info ----------------------------------------

CpuManagerMulti finished: Wed Dec 01 14:24:47


CpuManagerMulti (64-Bit) v20211118.0 Open Virt
Visit www.IMPERAS.com for multicore debug, ver


C:\Imperas\Demo\Platforms\quake\RV32>pause
Press any key to continue . . .
```

- This demo is RISC-V RV32, also runs on Imperas: RV32,RV64,MIPS32,ARM32,ARM64,OR1K
- Imperas virtual platform simulators can do sound, mouse/keyboard input, graphics output
- Imperas runs fast, real-time or faster…

Co-Design: HW and SW
Optimistic view of optimized design flow

The ideal goal:

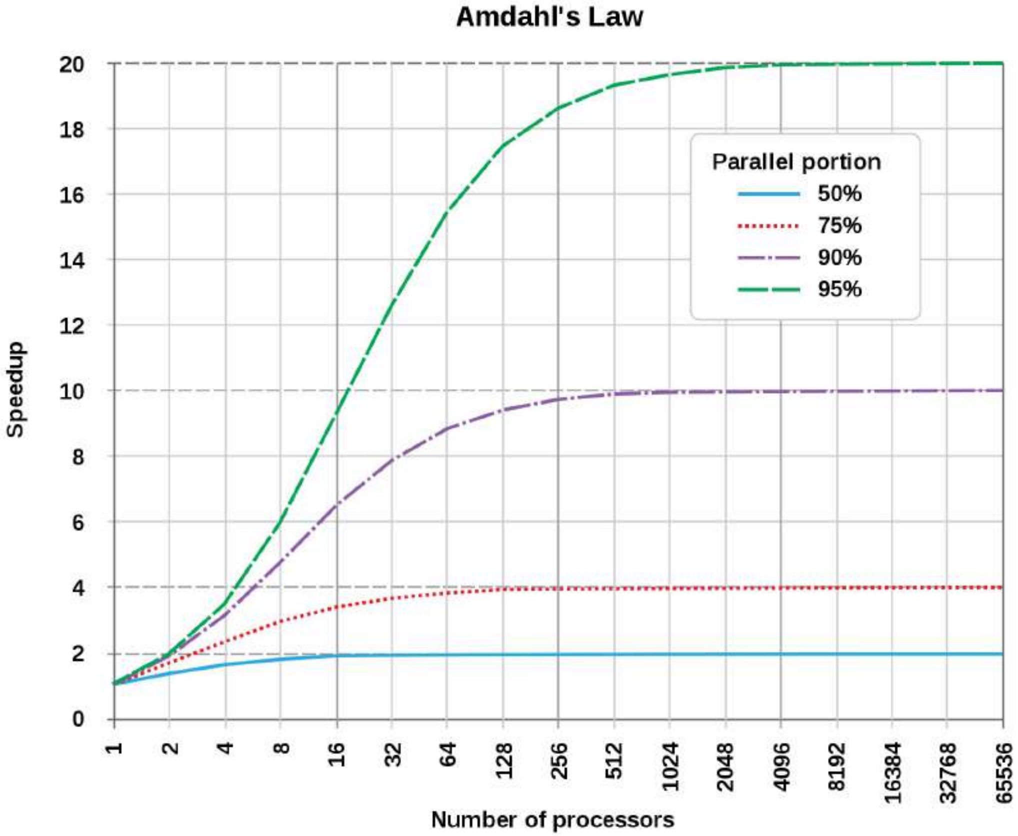
- Hardware optimized for the application requirements
- Software optimized for the hardware resources and efficiency
  - Repeat above steps…..

But what about the iteration time…..

- Hardware prototypes based on 1st order assumptions => estimate (guess ?)
  - Software partitioned for anticipated resources that are not yet implemented
    - Wait for hardware availability, wait to test full application, wait to debug….
      - Wait for software to test the prototype hardware (see step #1)
        - Slow iteration cycles => latest hardware runs last generation software a bit better

Amdahl's Law -
A guideline for multi-core efficiency

- IBM computer architect & entrepreneur
  - Left IBM when his ideas were rejected
  - Founded Amdahl computers:
    - Cheaper, faster, more reliable
    - IBM plug-compatible...
- Amdahl's law (1967) is used in parallel computing to predict the theoretical speedup when using multiple processors



$$S_{latency}(s) = \frac{1}{(1 - p) + \frac{p}{s}}$$

- $S_{latency}$ is the theoretical speedup of the execution of the whole task;
- s is the speedup of the part of the task that benefits from improved system resources;
- p is the portion of execution time that the part benefiting from improved resources originally occupied.

Why RISC-V?

- Optimized processor
  - Just the right features with just the right configuration
  - Flexible but standard extensions (= software ecosystem support)
  - Custom instructions (= application optimizations)

- Optimized platforms
  - Heterogeneous from multcore to clusters and beyond
  - Multiple optimized processors within a common framework
  - Custom hardware design with software compatibility

Modern Application Development Example for AI hardware accelerators

- Cloud based resources
  - Develop AI algorithm
  - Real word datasets (large scale models)
  - Need hardware acceleration for efficiency and deployment

- Virtual Prototype
  - Model hardware as abstraction for software development
  - Iterate design configurations at the speed of software
  - Functional test framework for processor hardware
  - SW and HW co-design

Example customer project

- Customer project
  - Full AI / ML engine
  - 150+ CPU cores
    - Over half with RISC-V Vector extension engine
- Imperas Reference Models and Virtual Platform provides environment for software stack development
- Simulation runs of software stack running in virtual platform take ~ 2hrs @ 500MIPS
  - Cross compiled software running on simulated CPUs
- Allows hardware platform configuration, re-configuration, architectural changes
  - Explore performance options
  - Runs real software (production binaries) – can see how it interacts with HW configuration
- **Running in Imperas virtual prototype more than a year before RTL commit**
  - Customer has SW and is looking to design HW to make it work the way they want…
- Also a by-product: kick-start SoC process by feeding models into HW DV at start

RISC-V => Freedom to innovate

- Design options now available at the point of use
  - End of the ‘one-size-fits-all’
  - Optimize with the right features and configuration options

- With RISC-V any developer can now optimize a custom processor
  - If you design it, you also need to test it!
  - Processor verification is migrating from a few specialist IP suppliers to all IP users that customize or optimize a RISC-V processor

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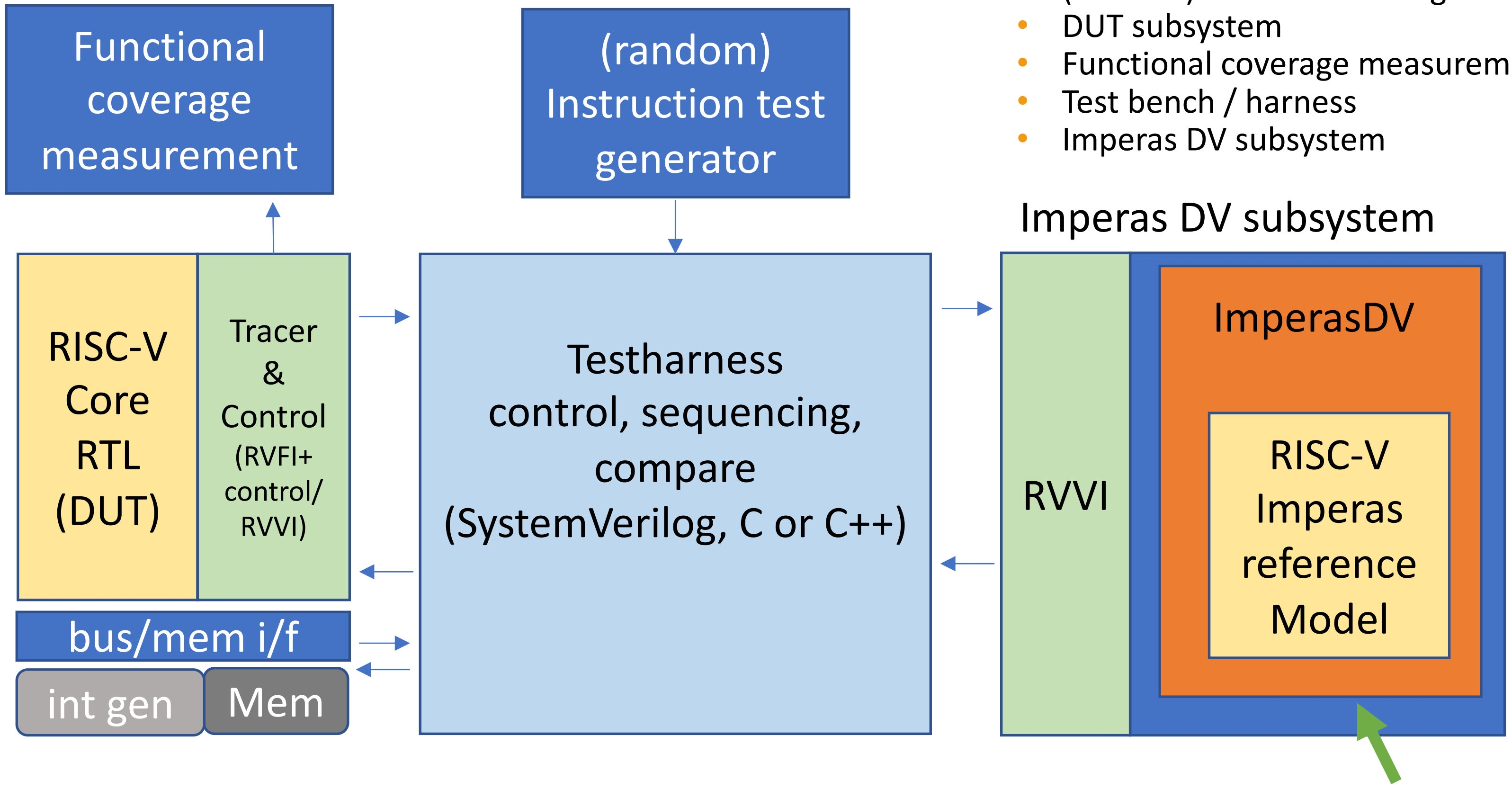

Functional coverage measurement

(random) Instruction test generator

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Tracer & Control (RVFI+ control/ RVVI)

bus/mem i/f

int gen

Mem

Testharness control, sequencing, compare (SystemVerilog, C or C++)

Imperas DV subsystem

RVVI

ImperasDV

RISC-V Imperas reference Model

Encapsulation of Imperas reference model

5 components of RISCV CPU DV

- (random) instruction test generator
- DUT subsystem
- Functional coverage measurement
- Test bench / harness
- Imperas DV subsystem

imperas
The leader in simulation solutions for RISC-V
RISC-V
VERIFICATION
ImperasDV
Quality Verification for the design freedom of RISC-V

- New solution to make it easy to verify RISC-V processor
- Works with SystemVerilog or C/C++ and Verilator
- sync-lock-step-compare and async-lock-step-compare

NOTE: ImperasDV can be used with SystemVerilog, C, C++, Verilator

RISC-V leading the next X years of Processors

- Open standard ISA
- Standard extensions and configurations
- Extensive software ecosystem support
- Flexibility with Compatibility

- Optimized hardware with software co-design
  - Start you next project with Virtual Prototypes
    - Why wait for hardware?

- 2022 prediction
  - Verification ecosystem supports mass adoption of RISC-V innovation

Thank you!

Stop by our booth in the RISC-V exhibit area or contact us at

info@imperas.com

www.imperas.com