



Software design: porting software to RISC-V using Imperas Virtual Prototypes

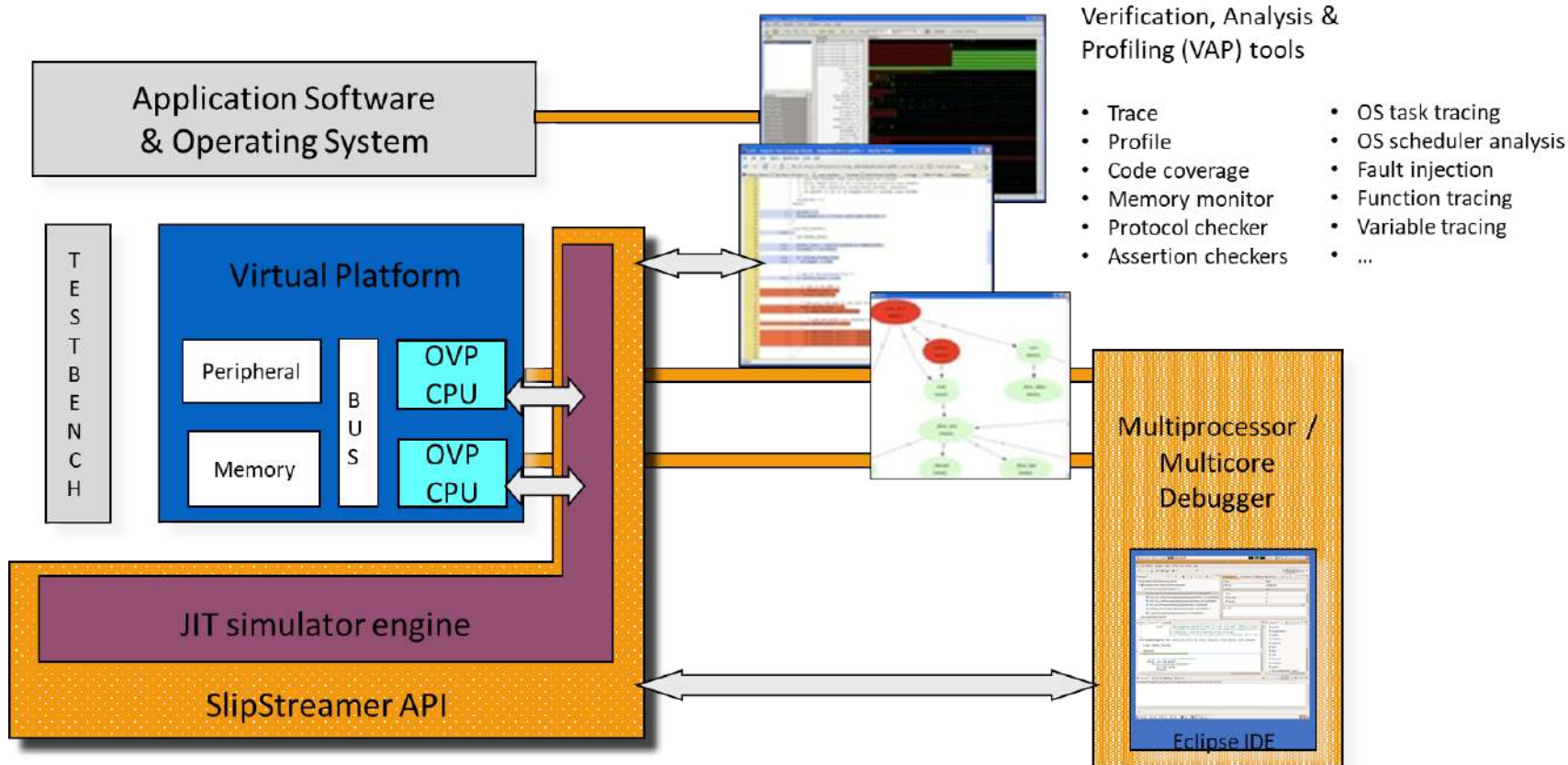
Kat Hsu & Manny Wright

Imperas Software Ltd.

RISC-V Summit, December 2021

- Modern SoC design flow: *“nobody designs a chip without simulation”*,
at Imperas we believe that:
“nobody should develop embedded software without simulation”
- Imperas develops simulators, tools, debuggers, modeling technology, and models to help embedded systems developers and SoC designers get their systems running... and their hardware verified
- 12+ years, self funded, profitable, UK based, team with much EDA (simulators, verification), processors, and embedded experience
- www.imperas.com
- www.OVPworld.org

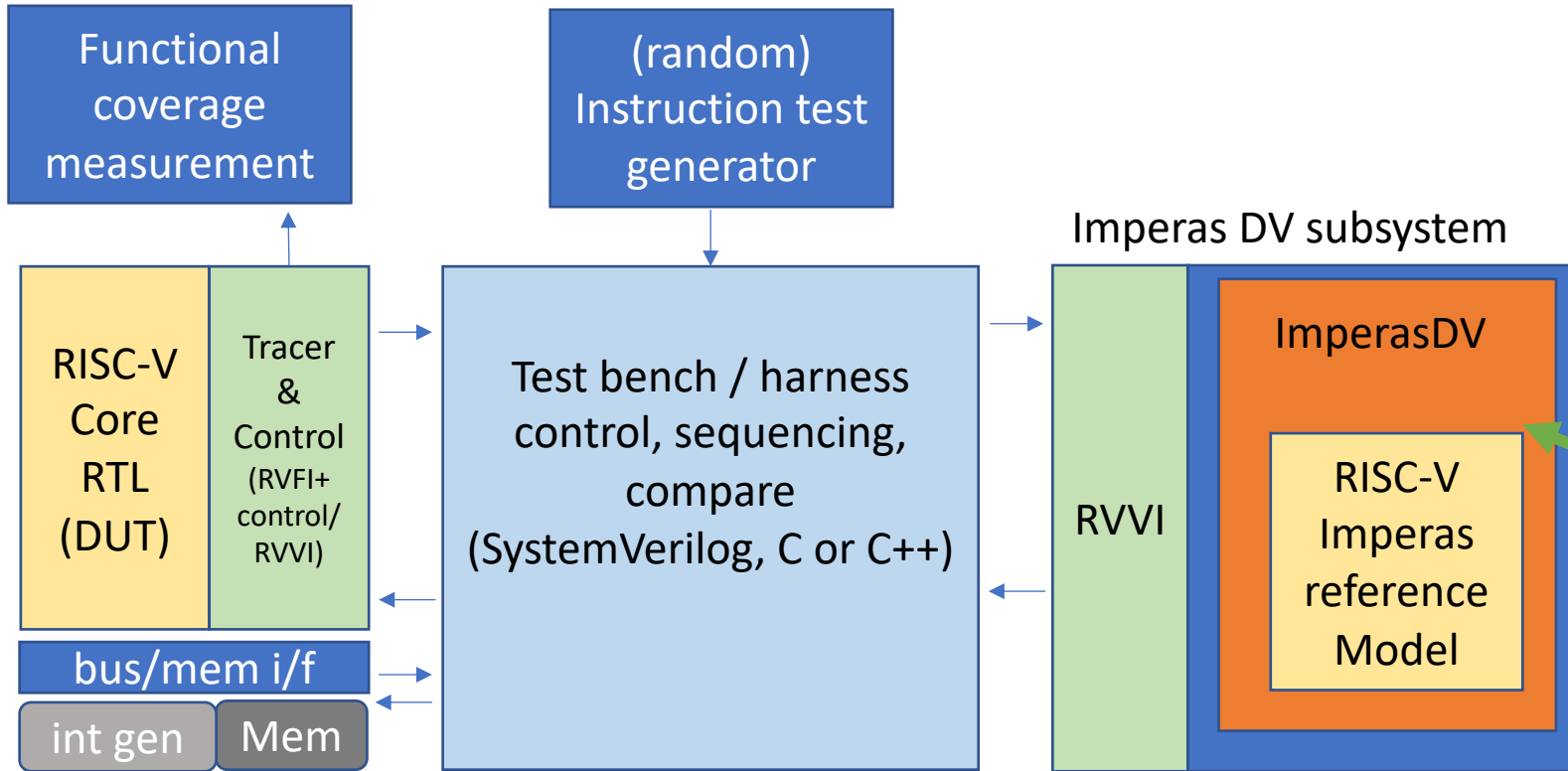
Simulation solutions for SW developers



- World class multicore simulator and full system emulator
- Library of advanced Verification, Analysis, Profiling tools
- Eclipse based Multiprocessor / Multicore debugger

Simulation solutions for HW Design Verification

ImperasDV – Launched at RISC-V Summit 2021



5 components of RISC-V CPU DV

- DUT subsystem with 'tracer'
- (random) instruction test generator
- Functional coverage measurement
- Test bench / harness
- Imperas DV subsystem

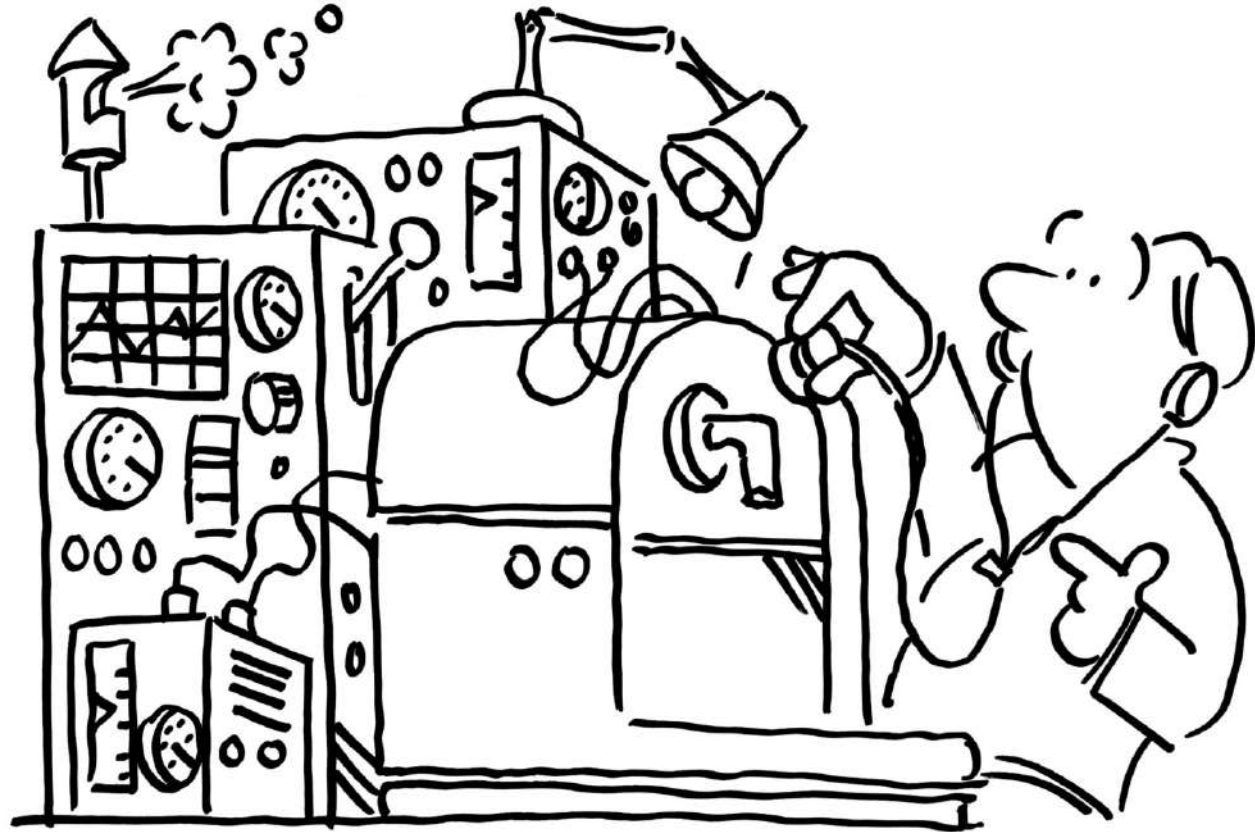
Encapsulation of Imperas reference model

NOTE: ImperasDV can be used with SystemVerilog, C, C++, Verilator

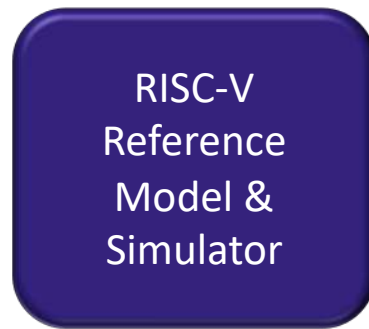
Key component is Reference Model



- RISC-V is highly configurable & extendable
 - 160... Questions ?
- So it can get a little complicated



Imperas is the Reference

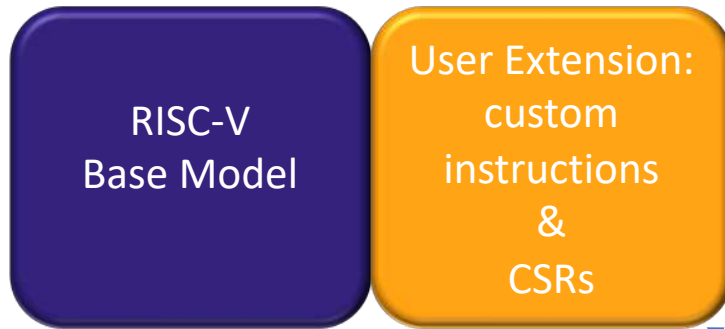


<http://www.imperas.com/riscv>

- Imperas provides full RISC-V Specification envelope model
- Industrial quality model /simulator of RISC-V processors for use in compliance, verification and test development
- Complete, fully functional, configurable model / simulator
 - All 32bit and 64bit features of ratified User and Privilege RISC-V specs
 - Vector extension, versions 0.7.1, 0.8, 0.9, 1.0
 - Bit Manipulation extension, versions 0.91, 0.92, 0.93, 1.0.0
 - Hypervisor version 0.6.1
 - K-Crypto Scalar version 0.7.1, 1.0.0
 - Debug versions 0.13.2, 0.14, 1.0.0
- Model source included under Apache 2.0 open source license
- Used as reference by :
 - Mellanox/Nvidia, Seagate, NSITEXE/Denso, Google Cloud, Chips Alliance, lowRISC, OpenHW Group, Andes, Valtrix, SiFive, Cudasip, MIPS, Nagra/Kudelski, Silicon Labs, RISC-V Compliance Working Group, ...

Imperas is used as RISC-V Golden Reference Model

Imperas Model extensibility



Imperas develops and maintains base model

- Base model implements RISC-V specification in full
- Fully configurable to select which ISA extensions
- Fully configurable to select which version of each ISA extension
 - Updated very regularly as ISA extension specification versions change
- Fully configurable for all RISC-V specification options
 - e.g. implemented optional CSRs, read only or read/write bits etc...

Imperas provides methodology to easily extend base model

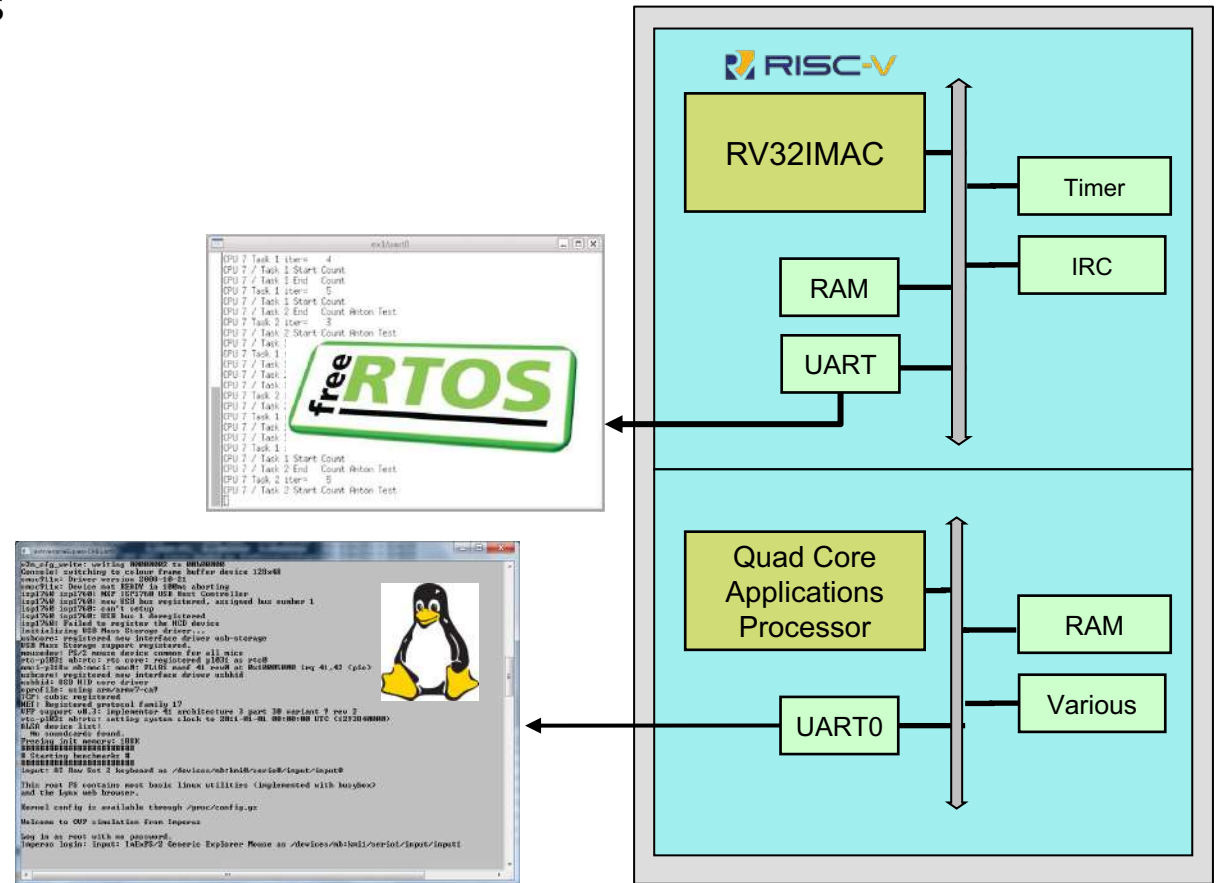
- Separate source files and no duplication to ensure easy maintenance
- Imperas or user can develop the extension
- User extension source can be proprietary

- Templates to add new instructions
- Code fragment for adding functionality
- 100+ page user guide/reference manual with many examples
 - Includes example extended processor model

Imperas model is architected for easy extension & maintenance

What is a Virtual Platform?

- The virtual platform is a set of instruction accurate models that reflect the hardware on which the software will execute
 - Could be 1 SoC, multiple SoCs, board, system; no physical limitations
- Run the executables compiled for the target hardware
- Models for individual components – interrupt controller, UART, ethernet, ... – are connected just like in the hardware
- Peripheral components can be connected to the real world by using the host workstation resources: keyboard, mouse, screen, ethernet, USB, ...
- High performance: 200 – 500 million instructions per second typical, or boots Linux in <10 secs



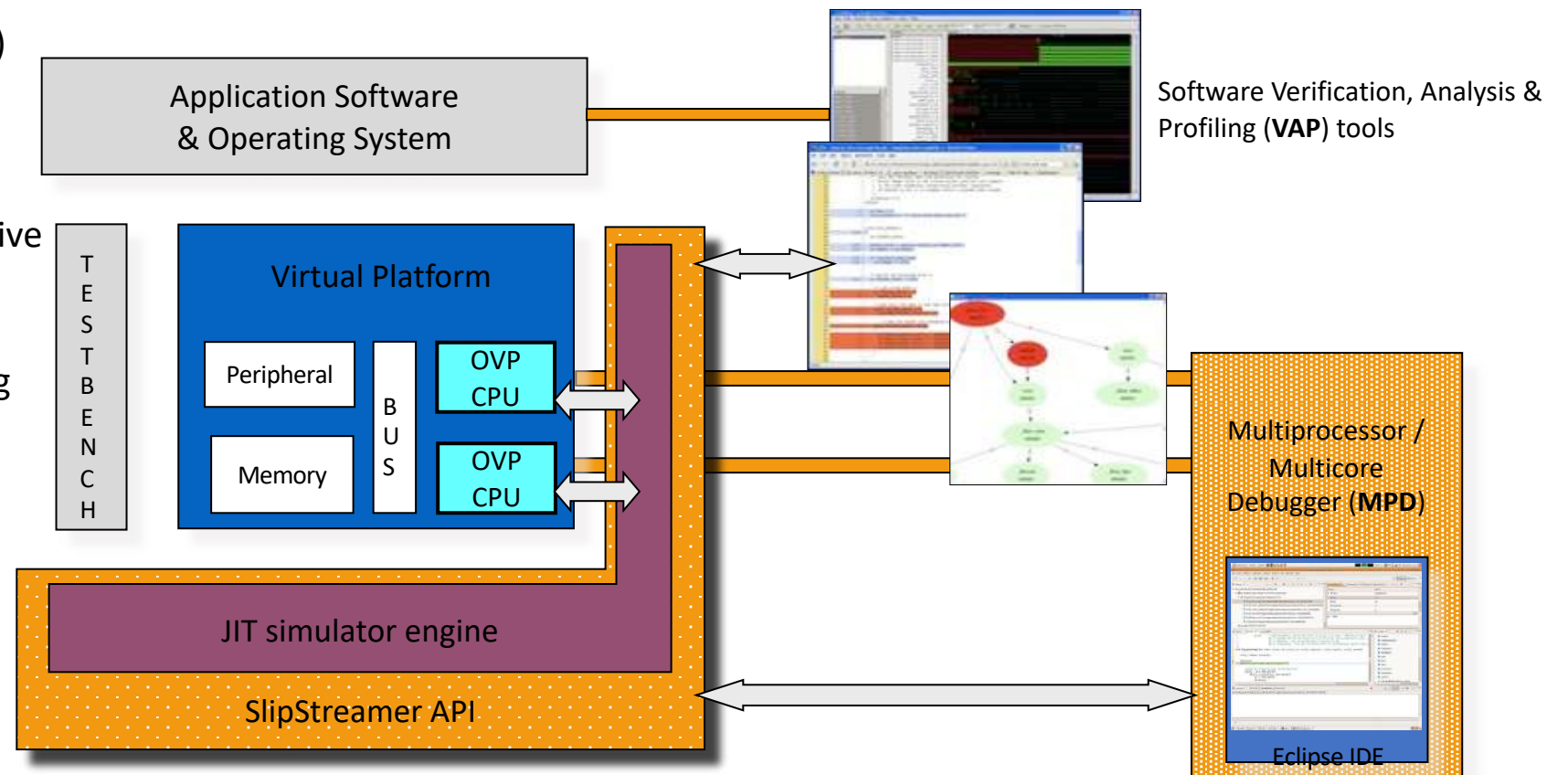
Extended Platform Kit with OS

Imperas Environment



Key technologies/differentiators:

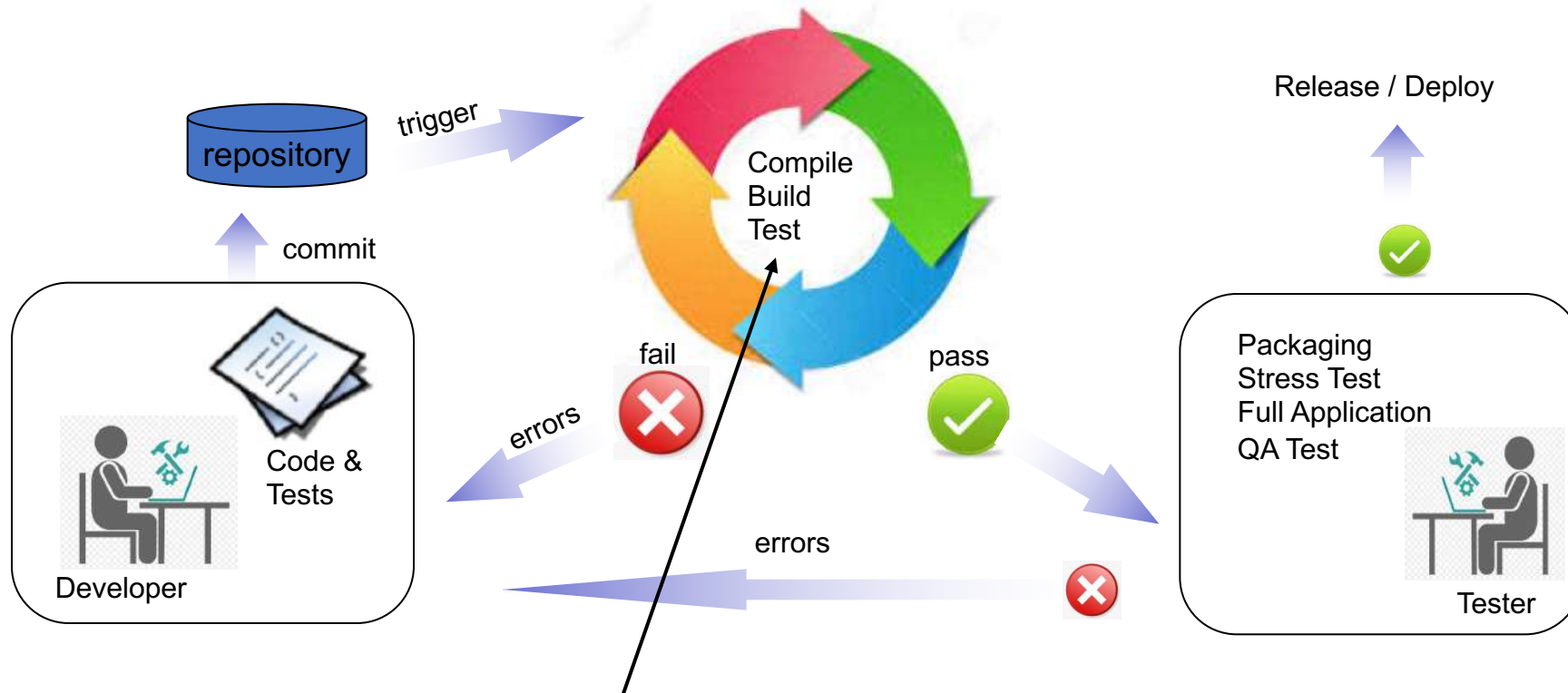
- OVP Fast Processor Models
 - Largest library of models (>275)
 - Highest quality
- Simulator engine
 - Highest performance
 - SlipStreamer API for non-intrusive tools
- Tools
 - MPD for platform-centric debug
 - VAP tools for comprehensive software analysis



Virtual platforms enable modern development methodologies, e.g. Agile

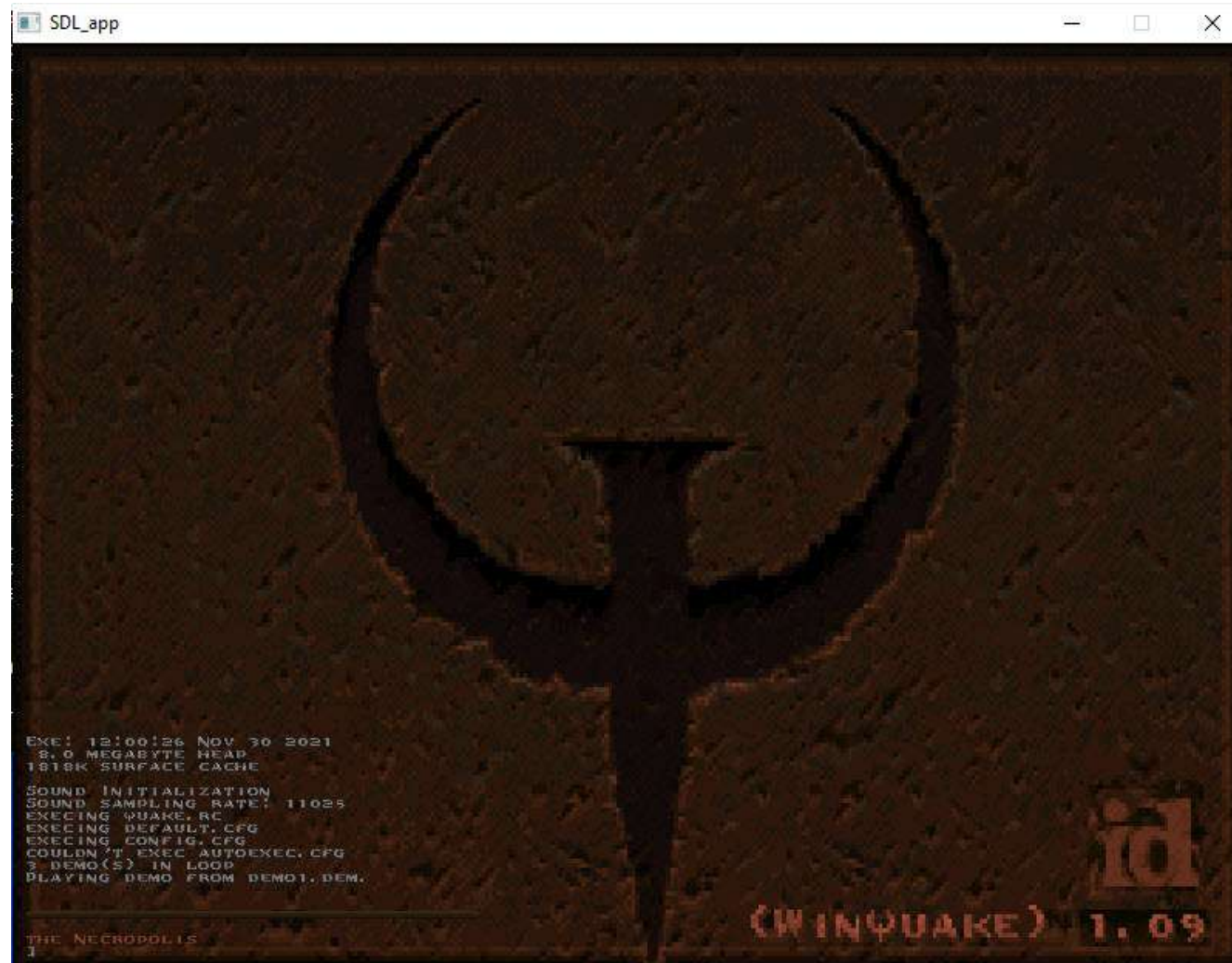


Continuous Integration Continuous Test (CICT)



Virtual platform based software simulation enables CICT

Id Games QUAKE – on RISC-V



Id Games QUAKE – on RISC-V



```
C:\Windows\system32\cmd.exe
You got the nails
You receive 25 health
You got the gold key
Simulator logfile
Info
Info -----
Info CPU 'iss/cpu0' STATISTICS
Info Type : riscv (RV32GC)
Info Nominal MIPS : 1000
Info Final program counter : 0x15d9a
Info Simulated instructions: 90,387,308,470
Info Simulated MIPS : 726.1
Info -----
Info
Info
Info -----
Info SIMULATION TIME STATISTICS
Info Simulated time : 90.39 seconds
Info User time : 105.45 seconds
Info System time : 19.86 seconds
Info Elapsed time : 124.48 seconds
Info -----
CpuManagerMulti finished: Wed Dec 01 14:24:47 2021

CpuManagerMulti (64-Bit) v20211118.0 Open Virtual Platform simulator
Visit www.IMPERAS.com for multicore debug, verification and analysis

C:\Imperas\Demo\Platforms\quake\RV32>pause
Press any key to continue . . .
```



- This demo is RISC-V RV32, also runs on Imperas: RV32,RV64,MIPS32,ARM32,ARM64,OR1K
- Imperas virtual platform simulators can do sound, mouse/keyboard input, graphics output
- Imperas runs fast, real-time or faster...

Id Games QUAKE – on RISC-V



Controls:

^

< >

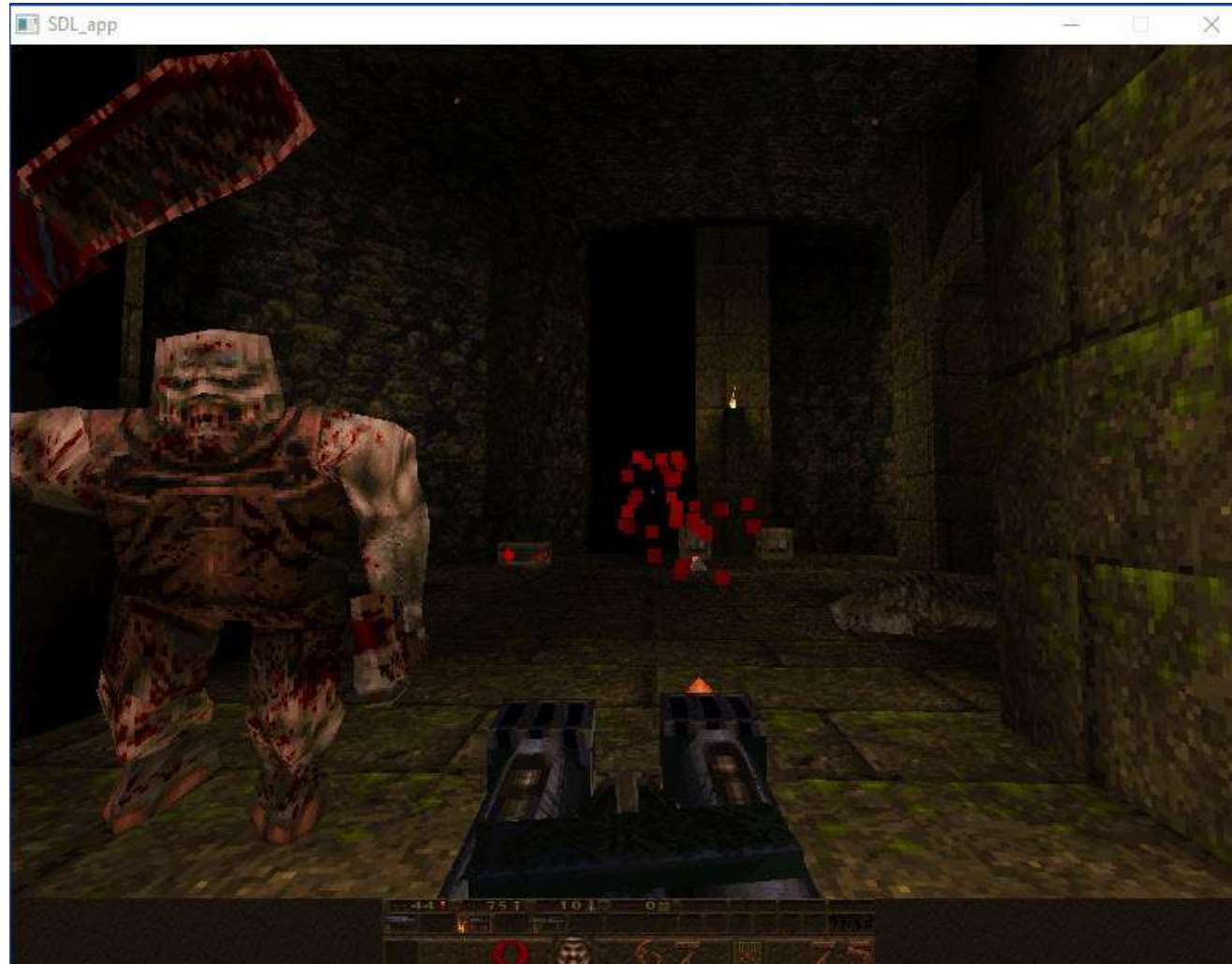
V

Ctrl

Esc

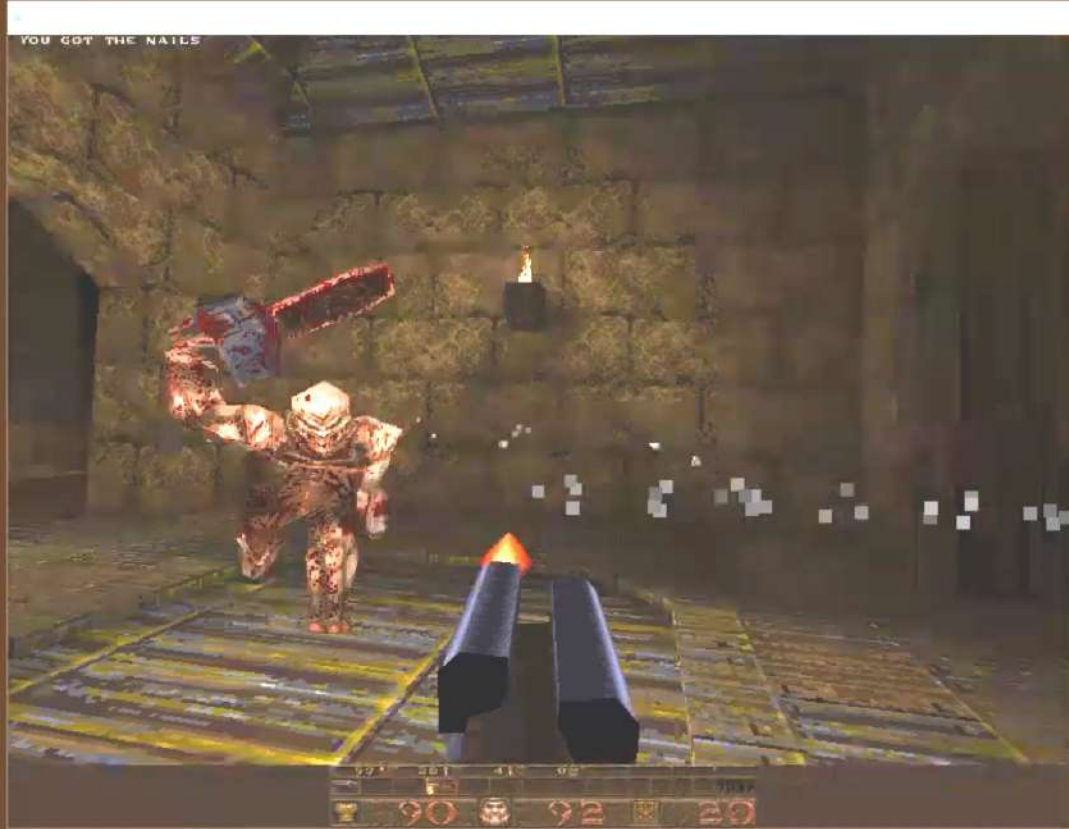
Quit

Y



Visit the Imperas Booth
at #B6 in the RISC-V Expo
area to see the demo and
play Quake on RISC-V!

Id Games QUAKE – on RISC-V



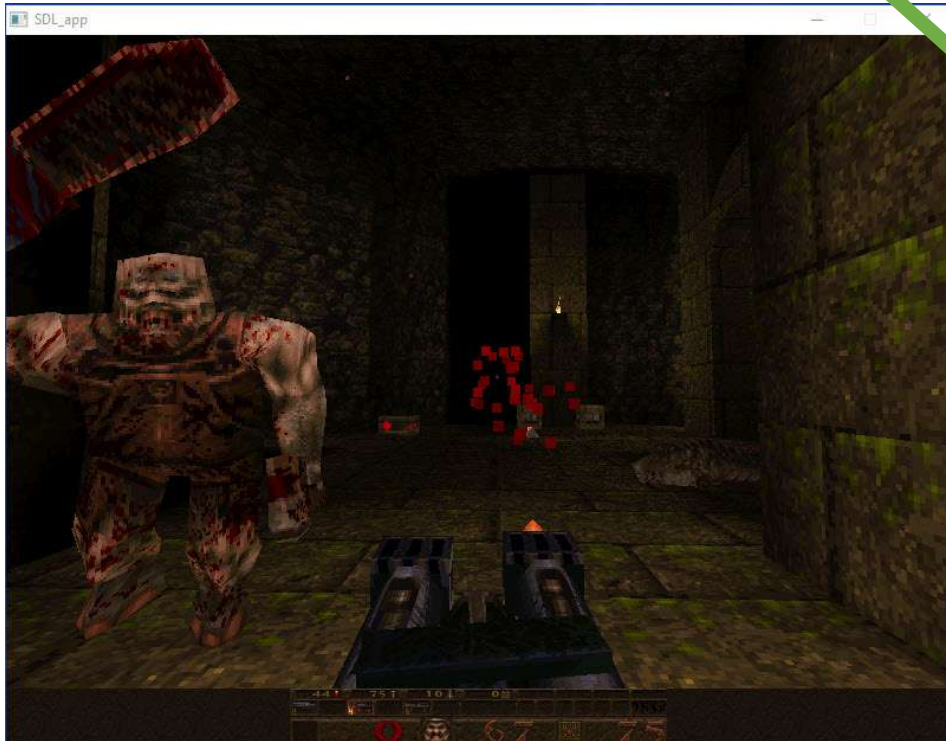
```
CA
You got the nails
You got the nails
You receive 15 health
You receive 15 health
You got the rockets
You get 2 rockets
You got the nails
You got the nails
You receive 25 health
You got the gold key
Playing demo from demo2.dem.
```

```
-----
@the Grisly Grotto
You got the shells
You got the shells
You got the nails
You got armor
You got the nails
You receive 25 health
You got the Super Nailgun
You got the nails
You get 2 rockets
You receive 25 health
You got the shells
You get 2 rockets
You got the nails
```

Id Games QUAKE – on RISC-V



Approx. 119 billion instructions
- with sound effects included



```
C:\Imperas\Demo\Platforms\quake\RV32>
You got the shells
You got the rockets
You get 2 rockets
Info
Info -----
Info CPU 'iss/cpu0' STATISTICS
Info Type : riscv (RV32GC)
Info Nominal MIPS : 1000
Info Final program counter : 0x15d9a
Info Simulated instructions: 119,127,027,700
Info Simulated MIPS : 731.3
Info -----
Info
Info -----
Info SIMULATION TIME STATISTICS
Info Simulated time : 119.13 seconds
Info User time : 159.45 seconds
Info System time : 4.52 seconds
Info Elapsed time : 162.89 seconds
Info -----

CpuManagerMulti finished: Wed Dec 01 19:46:42 2021

CpuManagerMulti (64-Bit) v20211118.0 Open Virtual Platform simulator from www.IMPERAS.com.
Visit www.IMPERAS.com for multicore debug, verification and analysis solutions.

C:\Imperas\Demo\Platforms\quake\RV32>pause
Press any key to continue . . .
```

Imperas Users Benefit From Improved Software Quality, and Reduced Schedules & Cost



- Key technologies:
 - 1) MultiProcessor Debugger (MPD) and Verification, Analysis and Profiling (VAP) tools
 - 2) Fastest simulator
 - 3) 300+ processor model library
 - 4) RISC-V processor verification solutions with **ImperasDV** see www.imperas.com/ImperasDV
- Imperas virtual platform solutions provide:
 - Controllability, observability, repeatability
 - Easy automation of testing (for continuous integration (CI) testing and regression testing)
 - Easy platform availability to software development and test teams
 - Additional (non-intrusive) tools such as memory monitoring, code coverage, fault simulation, OS-aware analysis and custom tools
 - Advanced software, platform, and processor verification

=> Schedule reduction (“*shift left*”) => “*why wait for hardware?*”



Thank you

OVPsim evaluation including
Quake demo (with next
release update) available at
www.OVPworld.com

info@imperas.com

www.imperas.com

www.OVPworld.org

Visit the Imperas Booth
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no monsters were harmed in this simulation