RISC-V Models & Tools for Verification, Software Development and Architectural Exploration

RISC-V Summit 2022: FutureWatch

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12 December 2022

The freedom, and not the free, is why RISC-V usage is growing so fast

Imperas and RISC-V

- Imperas founding team has background in Electronic Design Automation (EDA) tools, and FPGA and processor IP companies
- 2007: Imperas founding team saw the need for tools and methodology similar to EDA for software debug, test and analysis, based on software simulation
  - This required high quality models of the embedded processors
  - Self-funded the company, and built a business on virtual platform products serving Arm, MIPS, Renesas, etc. users
- In 2016, we realized the the RISC-V community would need RISC-V models for software development
- While there was, and still is a large demand for RISC-V models for software development, there is also a need for models of custom RISC-V cores, and a need for verification of RISC-V cores
- Imperas started working on RISC-V compliance, and then on processor verification, with RISC-V International and OpenHW Group, and customers such as Nvidia Networking, NSITEXE, MIPS, Codasip, Silicon Labs, and more
  - Imperas also developed riscvOVPsimPlus ISS, and made it freely available, supporting RISC-V processor DV for the complete RISC-V specification
- Now Imperas RISC-V processor models are used in almost every RISC-V project

Imperas RISC-V Customers and Partners

Most RISC-V processor projects use Imperas

Users

- Nvidia Networking (Mellanox)
- NXP
- Silicon Labs
- Seagate
- Nagravision
- Dolphin Design
- lowRISC (Ibex)
- EM Micro US
- Top 10 semiconductor company with embedded, GPU use cases
- Top-tier systems company (AI application)
- Largest automotive ADAS/AI company
- Startup building accelerator based on multiprocessor RV64
- Japanese government projects “TRASIO” and “RVSPF”
- Numerous universities around the world
- 100+ organizations using free riscvOVPsimPlus

Processor IP Partners

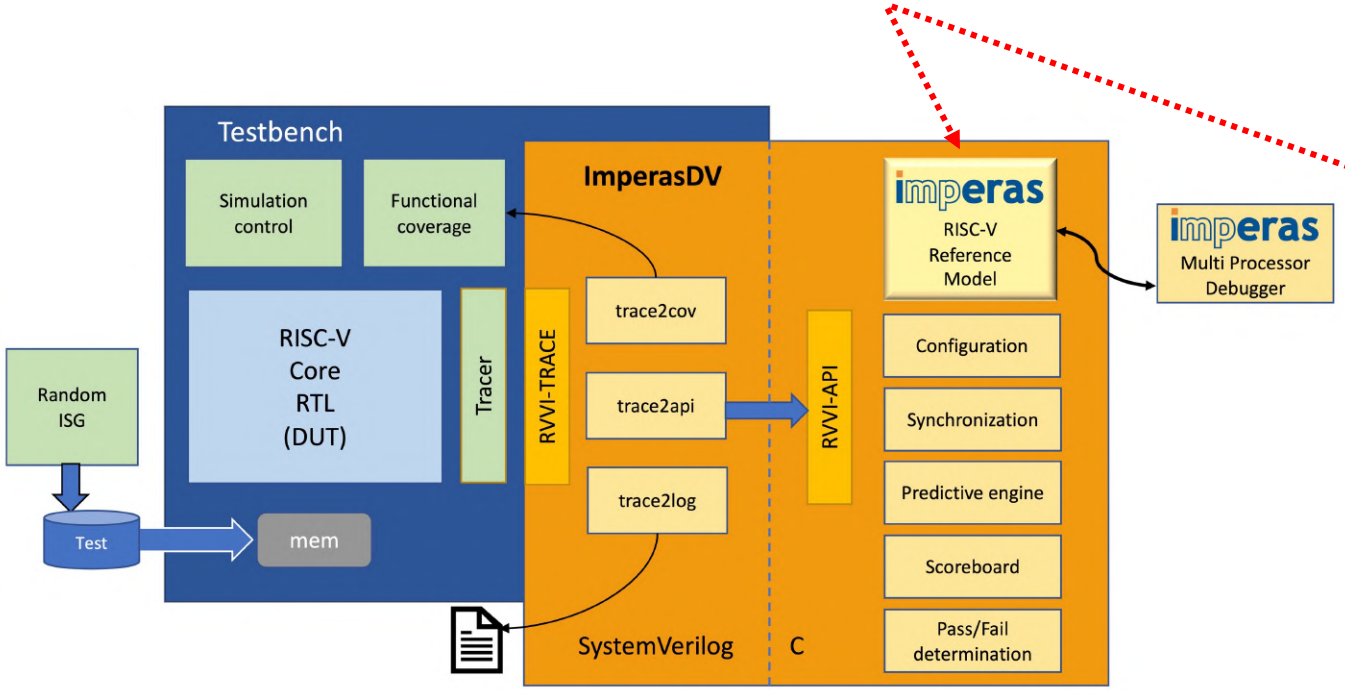
- RISC-V Intl
- Andes (processor IP vendor)
- Codasip (processor IP vendor)
- Intel FPGA (Nios-V processor IP)
- MIPS (processor IP vendor)
- Microchip (Microsemi FPGA Mi-V processor IP)
- NSITEXE (DENSO subsidiary)
- OpenHW Group (Imperas is chair of the verification task group)
- SiFive (processor IP vendor)

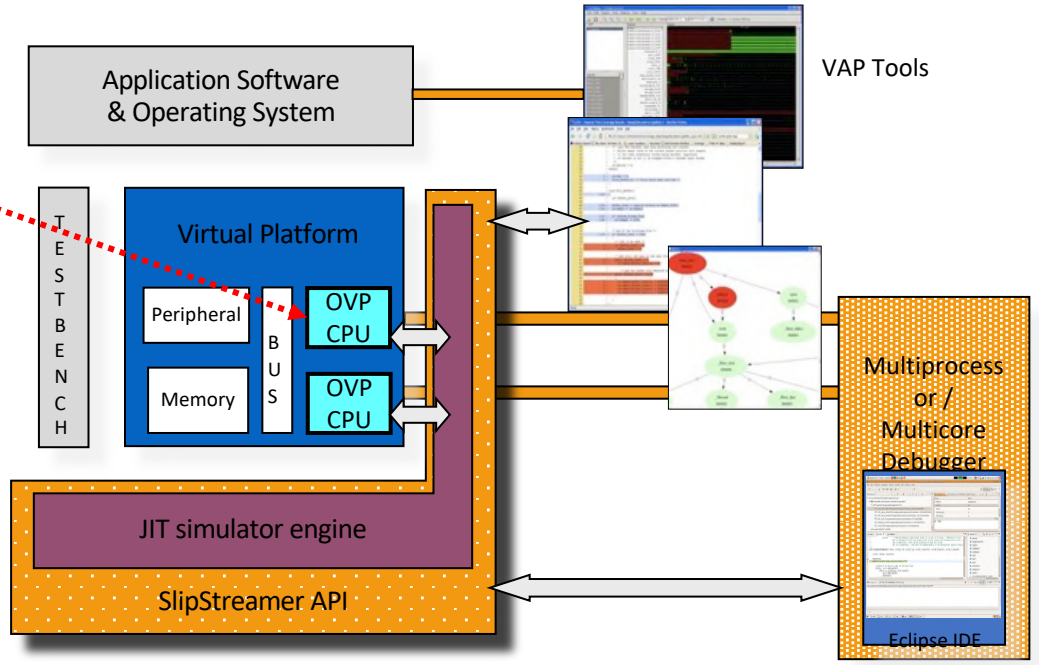
Tool Partners

- Breker
- Cadence (Palladium integration)
- Google (open source ISG)
- Intel (RISC-V Pathfinder IDE)
- Synopsys
- Valtrix (test generation tools)

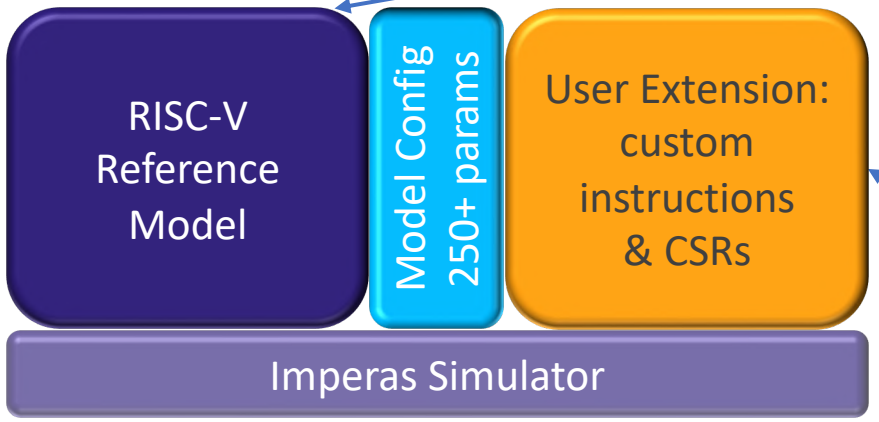
Imperas OVP RISC-V Models are used for Processor DV & SW Development

- Base model implements RISC-V specification in full
- Fully user configurable to select which ISA extensions/versions
- Imperas provides methodology to easily extend base model





Imperas Model Extensibility



- Separate source files and no duplication to ensure easy maintenance
- Imperas or user can develop the extension
- User extension source can be proprietary

Imperas develops and maintains base model

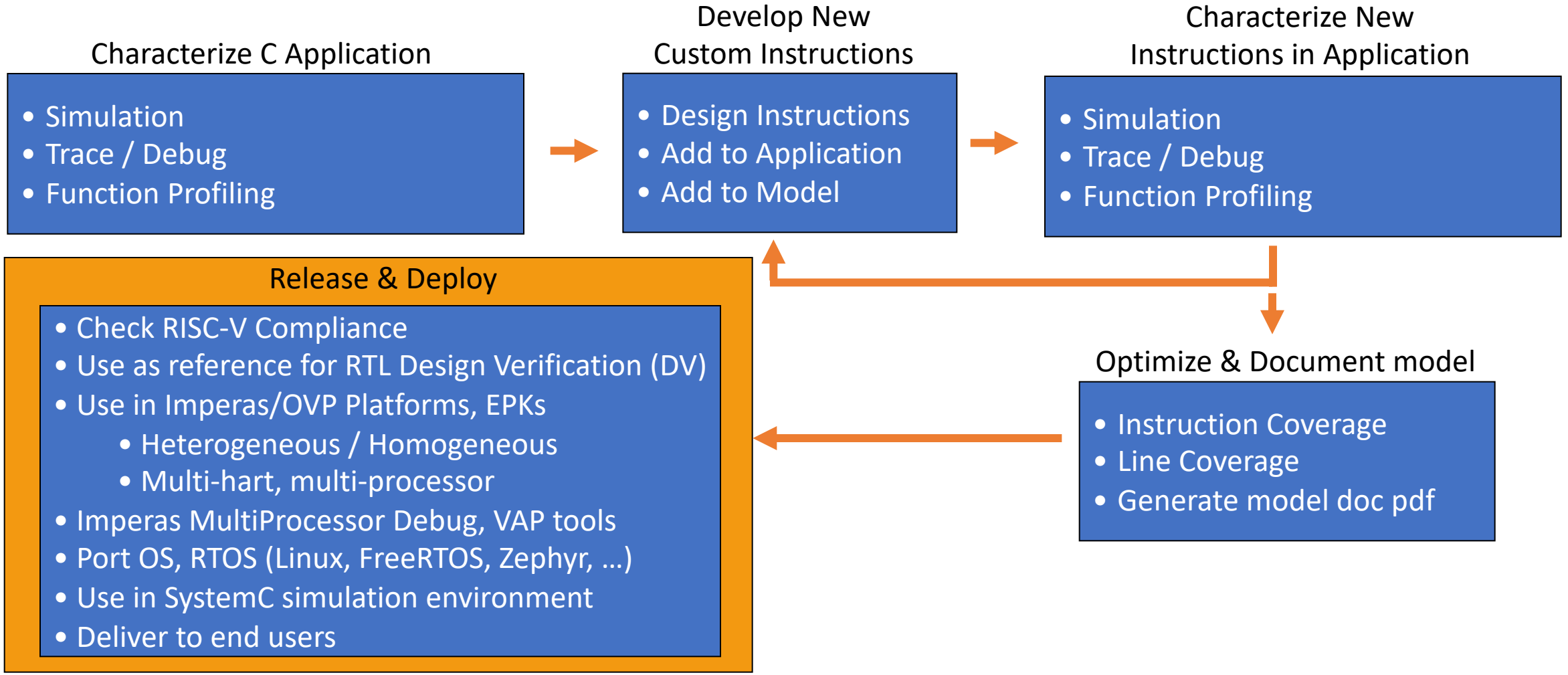
- Base model implements RISC-V specification in full
- Fully user configurable to select which ISA extensions
- Fully user configurable to select which version of each ISA extension
- Fully user configurable for all RISC-V specification options

Imperas provides methodology to easily extend base model

- Templates to add new instructions
- Code fragment for adding functionality
- 100+ page user guide/reference manual with many examples

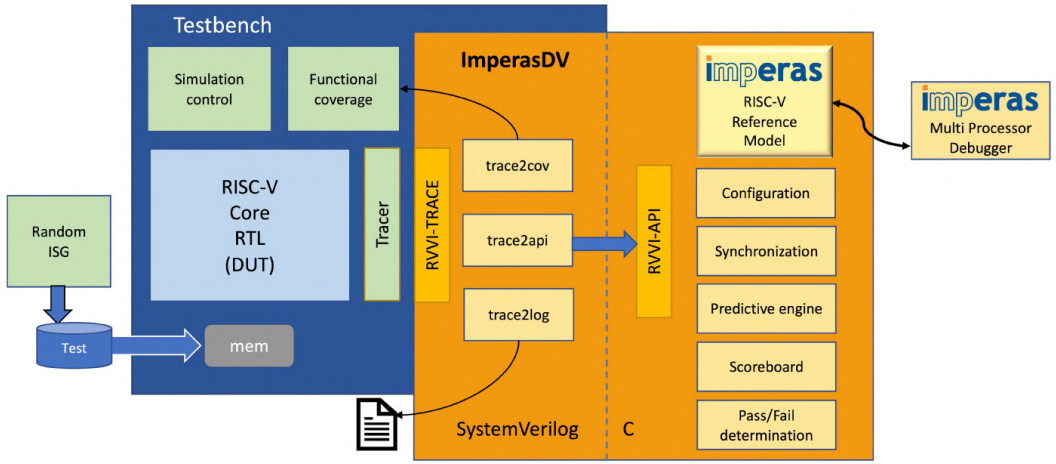
Imperas OVP model is architected for easy extension & maintenance

Flow to Add New Custom Instructions



Imperas RISC-V Processor DV Flow: Key Technologies are the RISC-V Reference Models and Verification IP

- Reference model needed for comparison of correct behavior
- Verification IP provides ease of use, saves time and resources
- RVVI standard provides communication between test bench and reference model subsystem
  - https://github.com/riscv-verification/RVVI

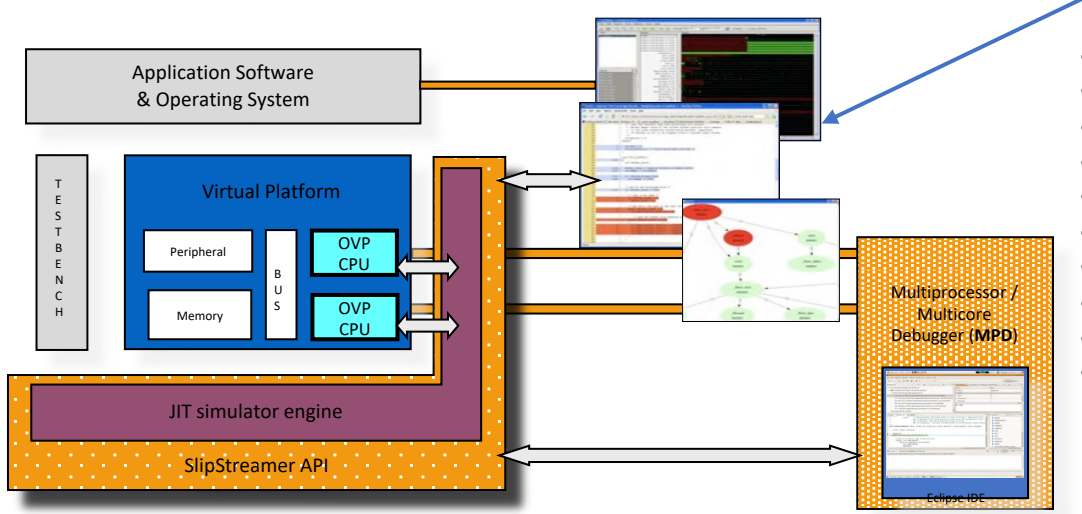


- Feature selection and design choices require serious consideration due to implications of every decision
  - Every addition dramatically compounds verification complexity
  - Adds schedule, resources, quality costs == big risks
- Before 2021, no off-the-shelf toolkit/products available for DV of processors … then came ImperasDV
- ***Imperas reference models + ImperasDV verification IP + RVVI = support for asynchronous-step-compare DV flow***
  - Needed to support features such as interrupts, privilege modes, Debug mode, multi-hart, multi-issue and OoO pipeline, …

Imperas Environment for Software Development, Architecture Analysis

Key technologies/differentiators:

- OVP Fast Processor Models
  - Most models
  - Highest quality
- Simulator engine
  - Highest performance
  - SlipStreamer API for non-intrusive tools
- Tools
  - MPD for platform-centric debug
  - VAP tools for comprehensive software analysis
  - Tools automatically work with custom features in models



Software Verification, Analysis & Profiling (**VAP**) tools

- Trace (instruction, function, variable, …)
- Profile
- Code coverage
- Memory monitor
- Protocol checker
- Assertion checkers
- Fault injection
- OS aware tools
- Timing estimation
- …

- Virtual platforms provide
  - Controllability, observability, determinism, ease of automation, ease of delivery, ease of maintenance
  - Shift left for software schedule, often the critical path to product delivery
  - Performance which enables comprehensive testing of many, many scenarios
- ***Virtual platforms are a must have for software/system of any complexity, or with quality/reliability/safety/security requirements***

Imperas News: Recent Presentations and Announcements

- Presentations
  - NSITEXE at RISC-V Tokyo Days, Nov 2022
  - Dolphin Design at DVCon Europe, Dec 2022
- Announcements
  - Andes
  - Imagination
  - ImperasDV
  - MIPS
  - NSITEXE
  - OpenHW

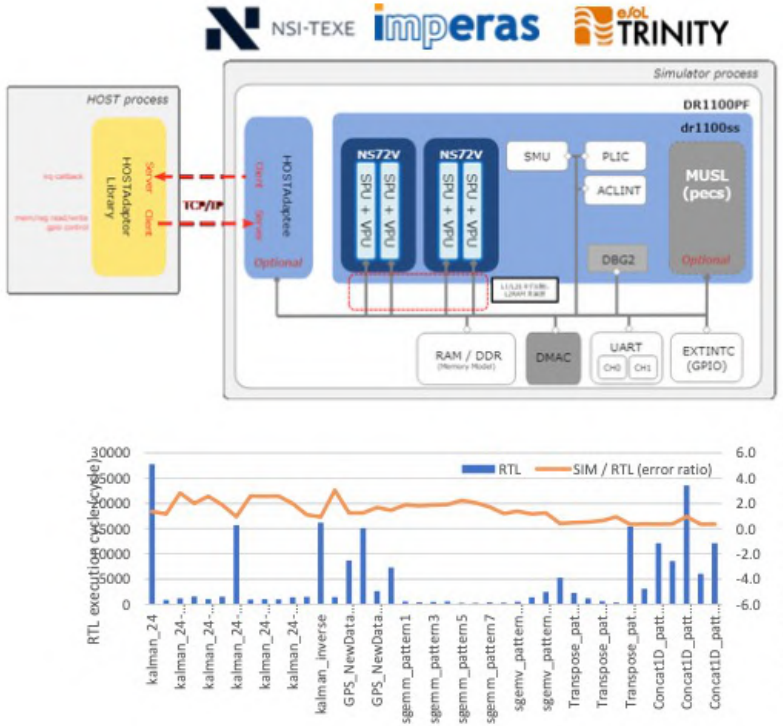
NSITEXE Using Imperas for Performance Estimation

(in addition to using Imperas for RISC-V processor DV and software development)

NS72 Performance Estimator

- Estimate rough performance gains from vector units
- Based on Imperas cpuDEV timing estimation capabilities
- Simulating pipeline, bus throughput and latency in a simplified manner
- Users can quickly estimate execution performance with reasonable accuracy without FPGAs, emulators, etc.

Akaria

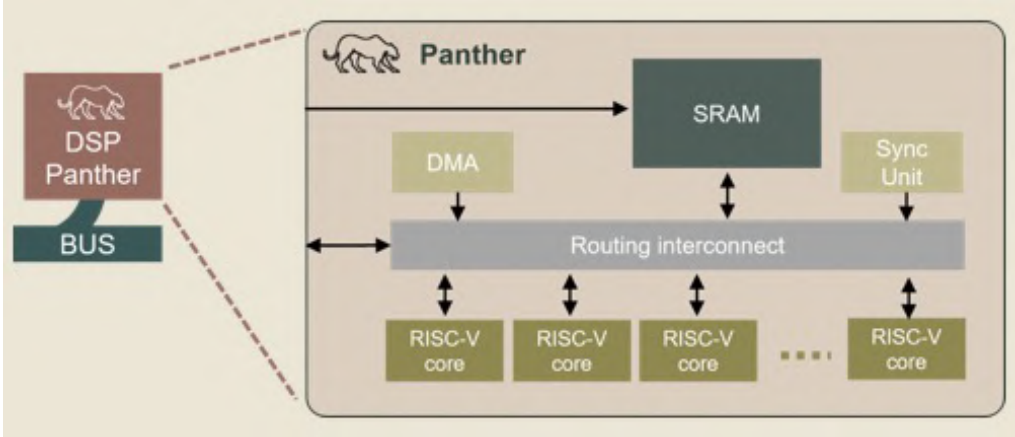


NSI-TEXE

From presentation at RISC-V Tokyo Days conference, Nov 2022

Development and Verification of RISC-V Based DSP Subsystem IP: Case Study – Dolphin Design Panther DSP

- Panther DSP: High throughput general purpose DSP, with extremely low power consumption
- Collaborating on verification of OpenHW CV32E40Pv2 RISC-V processor
- Also need performance estimation and software development using virtual platforms
- DVCon Europe summary
  - RISC-V processor DV – asynchronous-step-compare with Imperas reference model and verification IP – has been successfully used
  - Virtual platforms – software simulation – accelerate software development
  - The same RISC-V processor model can and should be used for both DV and software simulation

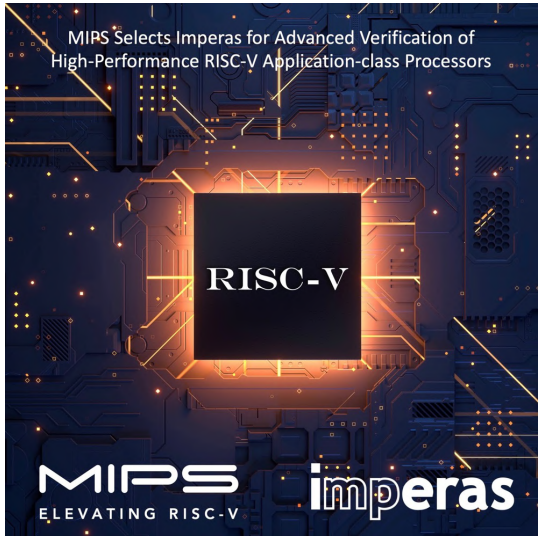


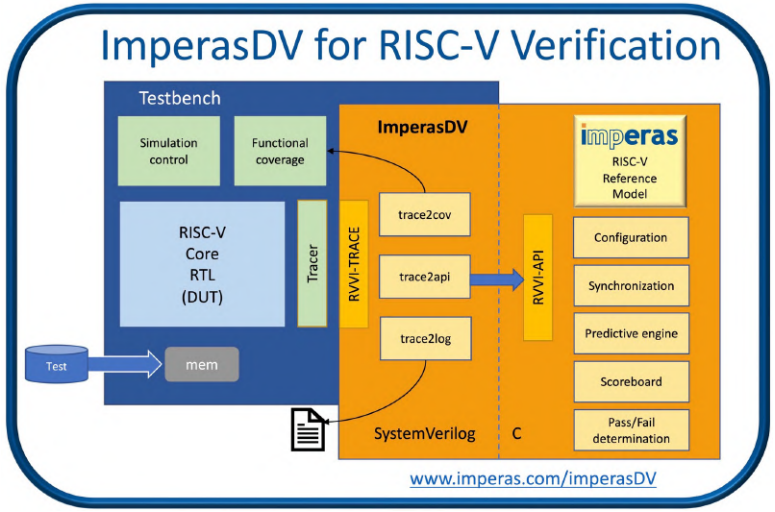
News for RISC-V Summit 2022

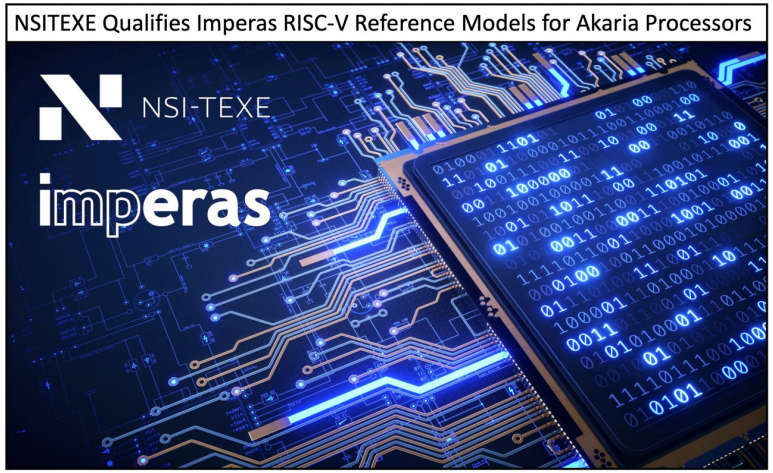
- Imperas and **Andes** collaborate to support RISC-V innovations – Nov 29th
- Simon Davidmann President & CEO of Imperas Software elected as Chair of the **OpenHW** Verification Task Group – Dec 5th
- **MIPS** Selects Imperas for Advanced Verification of High-Performance RISC-V Application-class Processors – Dec 7th
- Imperas and **Imagination** collaborate on providing virtual platform models for the Catapult RISC-V CPU family – Dec 8th
- Imperas releases new updates, test suites, and functional coverage library to support the rapid growth in RISC-V Verification – Dec 12th
- **NSITEXE** Qualifies Imperas RISC-V Reference Models for Akaria Processors NS72A, NS72VA, and NS31A – *Dec 13th (under embargo until 6am PST)*

News for RISC-V Summit 2022

imperas







Imperas Users Benefit From Improved Software & Hardware Quality, and Reduced Schedules & Cost

- Key technologies:
  1) MultiProcessor Debugger (MPD) and Verification, Analysis and Profiling (VAP) tools
  2) Fastest simulator
  3) 275+ processor model library
  4) RISC-V processor DV methodology and verification IP

- Imperas RISC-V solutions enable
  - Complete RISC-V processor verification
  - Comprehensive software testing
  - Schedule reduction (“*shift left*”)

Most RISC-V processor projects use Imperas

Thank you

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