Imperas Newsletter – August 2022

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The leader in RISC-V simulation solutions

News

Imperas announces the latest updates to RVVI (RISC-V Verification Interface) and welcomes the adoption by many leading RISC V processor developers

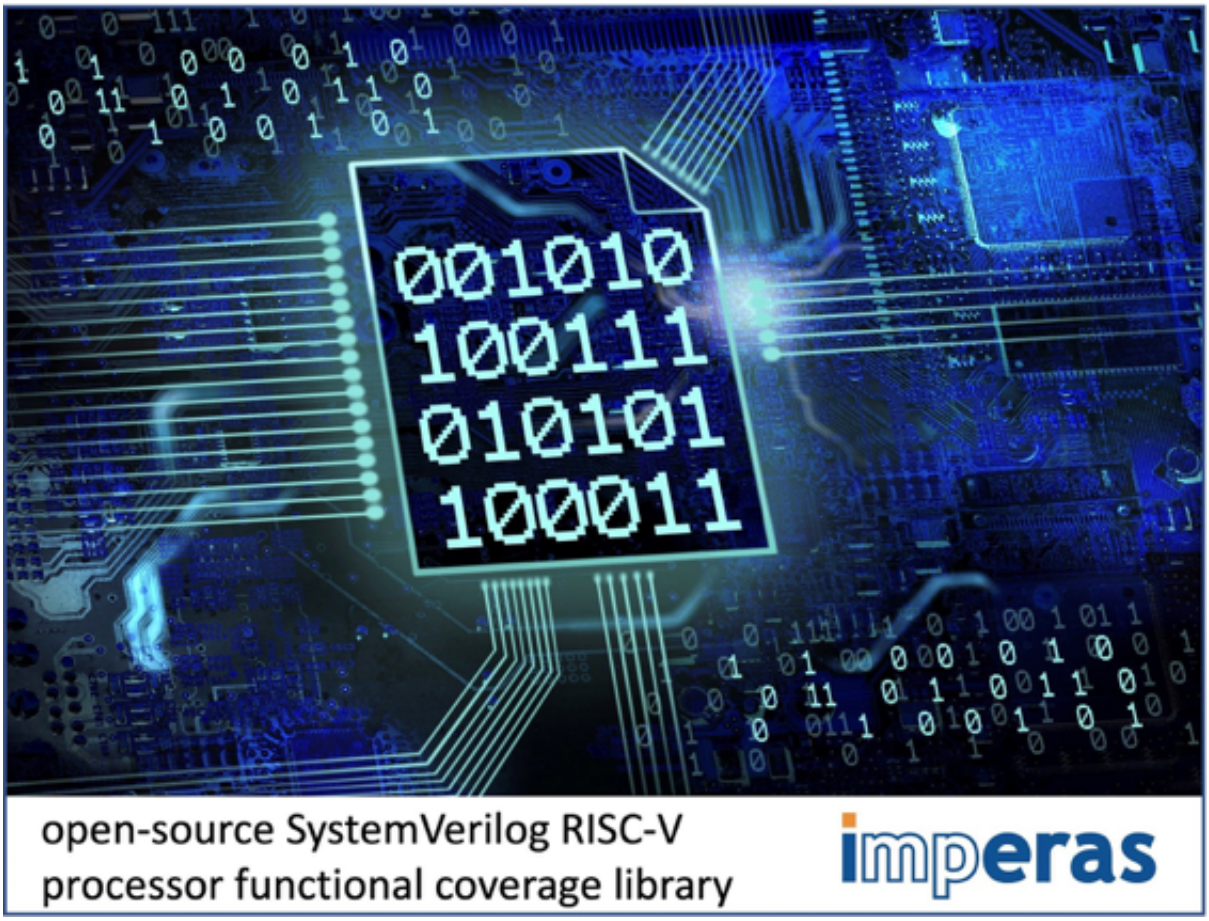
As a flexible framework, the RVVI (RISC-V Verification Interface) covers the needs of verification teams undertaking RISC-V processor functional verification and is a foundation for developing future guidelines, examples and verification IP. For more experienced DV engineers, RVVI offers the flexibility to cover the most complex verification challenges for advanced RISC-V designs. Some early supporters of RVVI include Codasip, NSITEXE (Denso), OpenHW Group, MIPS Technology, Silicon Labs, and Valtrix Systems, plus many others

yet to be made public.

“All the significant progress in processor innovation can be traced back to two fundamental building blocks: Abstractions and Standards,” said **Simon Davidmann, CEO at Imperas Software Ltd**. “Simulation of the latest designs with billions of transistors is achieved through abstraction, similarly the success of IP reuse has been enabled by standards. Now the emerging RISC-V verification ecosystem can build on the open standard RVVI flexible framework as a basis for verification IP and quality testing methods.”

The Imperas RISC-V processor verification technology already uses RVVI and is available now.

To find out more information, please contact us or follow this link.



Imperas releases the first open-source SystemVerilog RISC-V processor functional coverage library for RISC-V cores. The initial release is for RV32IMC, RV64 and other ratified extensions are under development and will also be released as part of the popular riscvOVPsimPlus package with a free-to-use permissive license from Imperas, which covers free commercial as well as

academic use.

“Functional coverage is fundamental to all modern processor verification plans; it marks the progress to project completion and release for prototype manufacture,” said **Allen Baum of Esperanto Technologies, Inc., and Chair of the RISC-V International Architecture Test SIG**. “The release of the Imperas SystemVerilog functional coverage library with a permissive free-to-use license will now benefit all RISC-V verification teams and complements the work of the RISC-V International Architecture Tests SIG.”

To find out more information, please contact us or follow this link.

Upcoming Events

Imperas to present at Andes RISC-V Con Taiwan - August 4, 2022

Andes RISC-V Con Hsinchu, Taiwan
When: Thursday, August 4th, 2022
Where: Both in-person and virtual attendance options
How: Free to attend but registration is required

Presentation:
Software-driven design optimizations with Imperas and Andes ACE
This talk will outline the architectural exploration process to optimize Andes ACE extensions for your applications using the Imperas reference models and analysis tools.
Speaker: Katherine (Kat) Hsu, Imperas Software Ltd
When: Thursday, August 4th, 2022 - TBD

For more information, or to set up meetings with Imperas at Andes RISC-V Con Taiwan, please email info@imperas.com

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Imperas to present at the SemIsrael Tech Webinar - September 13, 2022

Advanced RISC-V processor verification and methodologies
This talk will outline the latest advances in RISC-V functional verification to address the demands of high-reliability and automotive applications, including the innovations in processor designs with features such as: out-of-order pipelines, hardware multi-threading, multi-hart, custom extensions and advanced privileged modes, plus vector accelerators. Key updates will focus on functional coverage, Verification IP (VIP) and testbenches for asynchronous events, with examples from customers, partners and users at the forefront of RISC-V adoption.

Speaker: Larry Lapides, Imperas Software Ltd
When: September 13, 2022 – TBD (Tel Aviv, Israel)

For more information about SemIsrael Tech Webinar, please click here, or email info@imperas.com

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Imperas to present at the WISH Conference - September 13, 2022

The GSA (Global Semiconductor Alliance) has established its Women's Leadership Initiative (WLI) and the technical conference WISH (Women in

Semiconductor Hardware). The annual event features technical presentations on the latest updates for the design and development of semiconductor ICs and SoCs.

Open-source is a great price, but verification adds the real value
RISC-V adopters are exploring processor design freedoms enabled by the open standard ISA. These design freedoms are also driving the interest in open-source hardware. The OpenHW RISC-V cores are open-source, free is a great price but the real value is in the verification to industrial grade standards for commercial adoption. This talk will highlight the innovations in RISC-V processor verification that complements the design freedoms of the open standard ISA.

Speaker: Manny Wright – Imperas Software Ltd
When: September 13, 2022 10:50am – Santa Clara Convention Center

For more information about the WISH Conference, please click here, or to set up a meeting email info@imperas.com

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Imperas to present at RISC-V Virtual Career Fair - September 28, 2022

The RISC-V Virtual Career Fair is a virtual event that provides useful insights into opportunities and possibilities within the RISC-V community.

RISC-V: putting theory into practice with Imperas simulator, tools, and models
This talk will share some of the experiences of working in a company at the forefront of the RISC-V ecosystem in processor hardware functional verification and software development in an EDA start-up environment. Working at Imperas includes developing, supporting, marketing, and selling commercial tools for complex SoCs in AI, automotive, datacenter, industrial, and high-reliability applications.

Speaker: Larry Lapides – Imperas Software Ltd
When: September 28, 2022 - virtual event in California timezone

For more information about the RISC-V Virtual Career Fair, please click here.

Video Interviews

EDA Café's Sanjay Gangal interviews **Larry Lapides at Imperas Software** to find out the latest developments of RISC-V. Click here or on the image above to watch the interview in full.

Embedded World 2022 Featured Videos

Calista Redmond, CEO, RISC-V International speaks to
Larry Lapides, Imperas Software Ltd

Introduction to RISC-V Processor Verification
Larry Lapides, Imperas Software Ltd

Running Quake on RISC-V with Virtual Platforms
Kevin McDermott, Imperas Software Ltd

Getting Started with RISC-V Custom Instructions
Larry Lapides, Imperas Software Ltd

In the News

[RISC-V Announces First New Specifications of 2022, Adding to 16 Ratified]

in 2021

RISC-V International announced its first four specification and extension approvals of 2022 – Efficient Trace for RISC-V (E-Trace), RISC-V Supervisor Binary Interface (SBI), RISC-V Unified Extensible Firmware Interface (UEFI) specifications, and the RISC-V Zmmul multiply-only extension. The news builds on momentum from 2021, in which 16 specifications representing more than 40 extensions were ratified…

To read the full **RISC-V International** announcement, click here.

Embedded World 2022: RISC-V developments

Embedded World 2022 was the place to be for the latest RISC-V developments. Innovations ranged from Think Silicon's first RISC-V–based GPU, targeting 32-bit SoCs, to the OpenHW Group's new open-source RISC-V development kit, based on the OpenHW CORE-V microcontroller (MCU). This all happened as a backdrop to RISC-V International's first specification and extension approvals for 2022...

To read the full **Electronic Products** article by **Gina Roos**, click here.

Europe steps up as RISC-V ships 10bn cores - Embedded World 2022 news round-up

It may come as a surprise that over 10 billion RISC-V processor cores have shipped. After all, it took ARM 17 years to reach that milestone in 2008, and RISC-V could be considered to be in its infancy with a consensus that the eco-system still needs to evolve, particularly around security. These two factors result from the open standard approach to an inherently custom technology. The open standard is key, Calista Redmond, CEO of RISC-V International told eeNews Europe at the recent Embedded World exhibition...

To read the full **eeNews Europe** article by **Nick Flaherty**, click here.

A quick look at the DAC 2022 conference program

The Design Automation Conference is back to its usual summer timeframe –

again at the Moscone Center in San Francisco – with over one hundred exhibitors and a rich conference program that covers a wide range of topics including artificial intelligence, autonomous systems, RISC-V, security, embedded systems and more. Here we will briefly highlight some of the conference content more directly related to EDA, referring readers to the conference program for the detailed schedule…

To read the full **EDACafé** article by **Roberto Frazzoli**, click here.

Open Standard RISC-V Verification Interface (RVVI) for SOC testing

The **RVVI (RISC-V Verification Interface)** flexibility supports the full range of RISC-V specifications and features that can be adopted with increasing levels of complexity for designs with privilege modes, vector extensions, out-of-order pipelines, multi-threading, multi-hart, plus user-defined custom instructions and extensions. RVVI supports the innovation of RISC-V with the flexibility required for verification IP and reuse as DV teams scale up to support the rapid growth in RISC-V verification projects…

To read the full **eeNews Europe** article by **Nick Flaherty**, click here.

ARTICLES FROM SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

Heterogenous Integration Creating New IP Opportunities

The design IP market has long been known for constant change and evolution, but the industry trend toward heterogenous integration and chiplets is creating some new challenges and opportunities. Companies wanting to stake out a claim in this area have to be nimble, because there will be many potential standards introduced, and they are likely to change quickly as the industry explores what is required for various forms of integration…

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

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riscvOVPsim and riscvOVPsimPlus - LATEST NEWS

The latest Imperas and OVP release at the Open Virtual Platforms website.

For an introduction to RISC-V the free single-core envelope model, called **riscvOVPsim**, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the latest ratified specifications including Bit Manipulation, Crypto (scalar) and Vectors.

The latest version is available via GitHub here.

The free enhanced **riscvOVPsimPlus**, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the OVP website here.

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