Imperas Newsletter – December 2021

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The leader in RISC-V simulation solutions

Watch for our announcement on RISC-V verification that Imperas will reveal during the RISC-V Summit Keynote next week.

Events

RISC-V® Summit

Imperas at the RISC-V Summit, December 6-8 2021

As a proud Diamond sponsor of the 2021 RISC-V Summit, Imperas will be delivering keynote talks and presentations.
In addition, stop by the Imperas booth on the RISC-V Pavilion, or the hybrid on-line event platform, and see all the latest demonstrations of Imperas simulation technology and virtual platforms / prototypes for RISC-V software development, and RISC-V processor verification.
For more information, or to schedule a demonstration session at the RISC-V Summit 2021, please contact the Imperas team via info@imperas.com.

Day #1 Keynote:
Are the RISC-V design freedoms leading to RISK in Verification quality?
Speaker: **Larry Lapides, Imperas Software**
When: **Monday, December 6 at 1:40pm (PST)**

Lightning talk:
Open-Source RISC-V Cores with Industrial strength verification
Speaker: **Simon Davidmann and Lee Moore, Imperas Software**

When: **Monday, December 6 at 10:45am (PST)**

Day #3 Keynote:
Is hardware/software co-design for applications now a reality with RISC-V?
Speaker: **Kevin McDermott, Imperas Software**
When: **Wednesday, December 8 at 1:50pm (PST)**

Demo Theatre:
Brief introduction to the 5 levels of RISC-V processor verification
Speaker: **Larry Lapides and Lee Moore (Demo), Imperas Software**
When: **Tuesday, December 7 at 10:20am (PST)**

Demo Theatre:
Software design: porting software to RISC-V using Imperas Virtual Platforms
Speaker: **Katherine (Kat) Hsu and Manny Wright (Demo), Imperas Software**
When: **Wednesday, December 8 at 10:20am (PST)**

For more information, or to set up meetings with the Imperas team during the summit, please contact info@imperas.com.

Click here for more information about the RISC-V Summit 2021.

DESIGN AUTOMATION CONFERENCE

FROM CHIPS TO SYSTEMS — LEARN TODAY, CREATE TOMORROW

Imperas at Design Automation Conference, December 5-9 2021

Imperas will be participating at DAC on the RISC-V Pavilion for in-person demonstrations and discussions with the Imperas team. Presentations will also be featured in both the DAC and RISC-V Summit technical conferences, which are co-located for 2021.

RISC-V processor verification methodology with dynamic testbench for asynchronous events

Speaker: **Man Wai (Manny) Wright, Imperas Software**
When: **Monday, December 6th, 5:00pm (PST)**
Where: **Level 2 - Exhibit Hall**
Event Type: **Designer, IP and Embedded Systems**
Poster Networking Reception

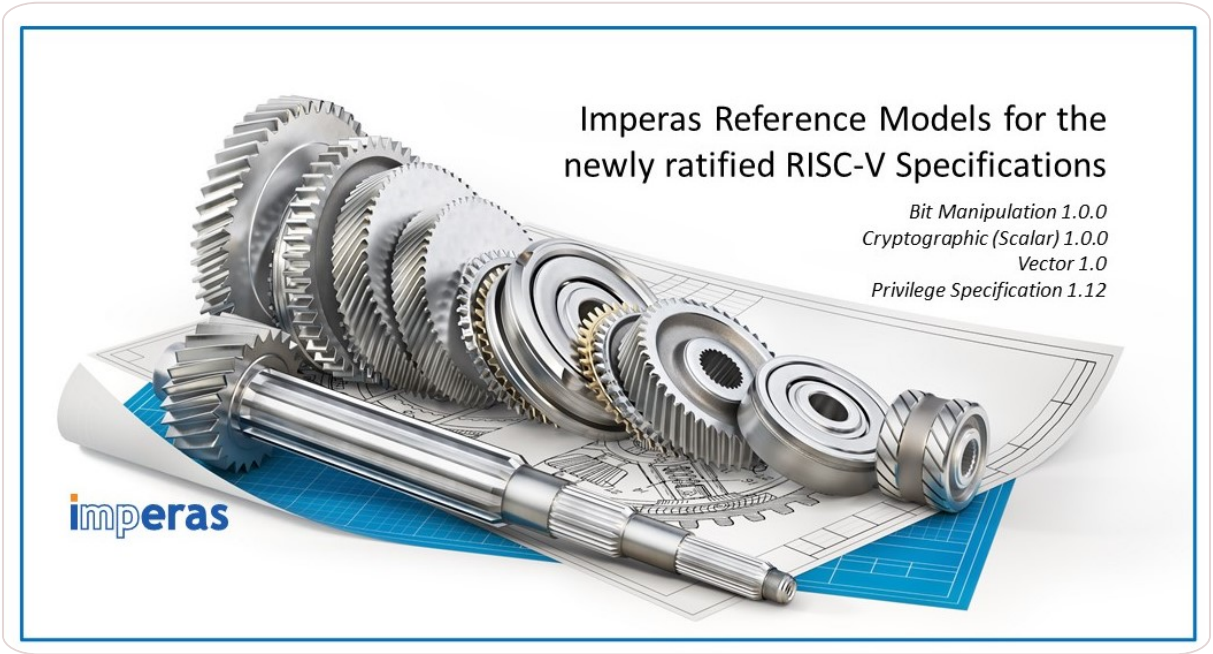
SoC Architectural Exploration for AI and ML accelerators with RISC-V

Speaker: **Katherine (Kat) Hsu, Imperas Software**
When: **Monday, December 6th, 11:10am (PST)**
Where: **Conference Room #2010-2012**
Event Type: **Designer, IP and Embedded Systems Track**

For more information, or to schedule a demonstration session at DAC 2021, please contact the Imperas team via info@imperas.com.

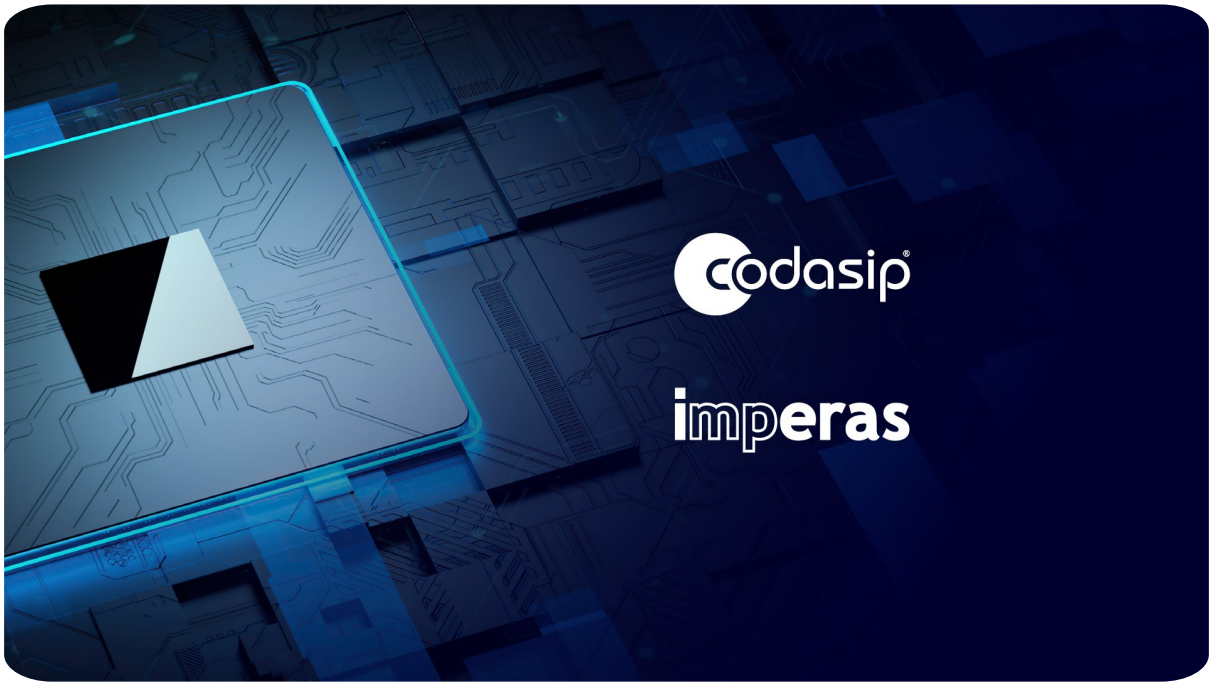
Click here for more information about DAC 2021

Latest News



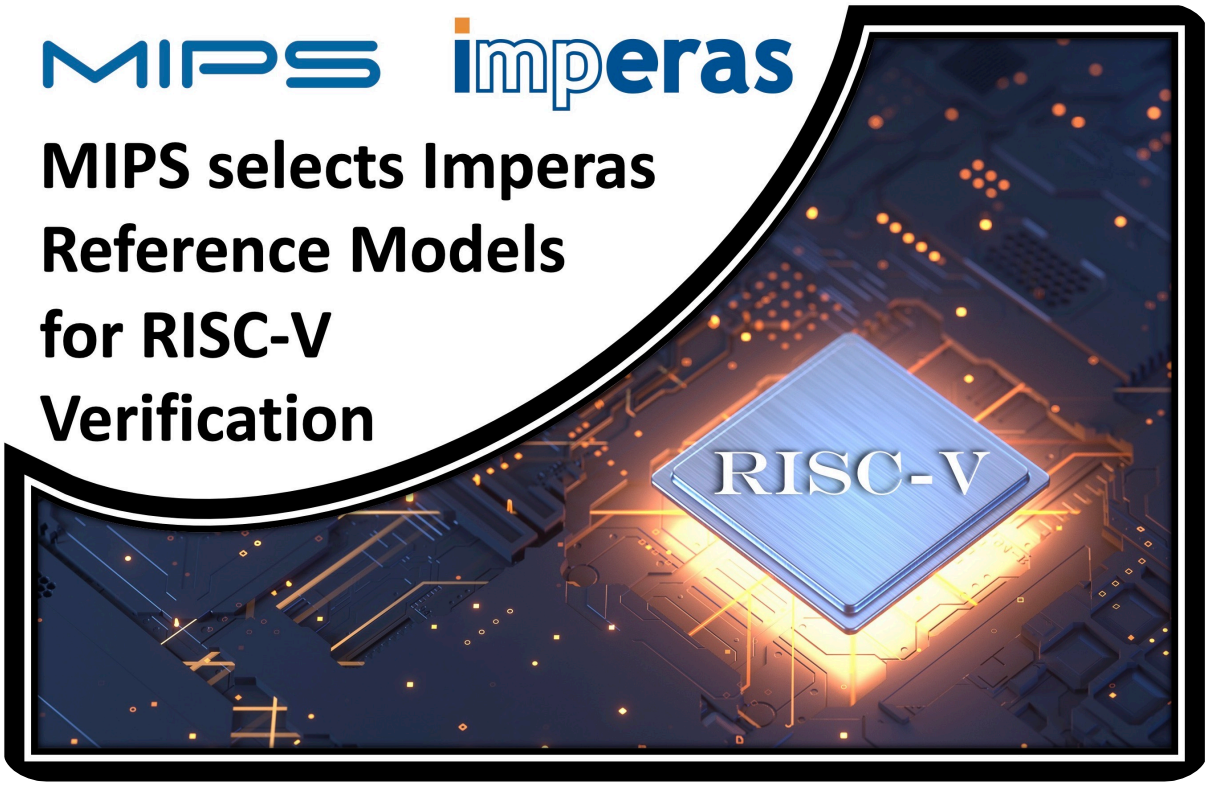
4Q2021 release of Imperas simulator and reference models supports latest RISC-V Extensions for Bit Manipulation 1.0.0, Cryptographic (Scalar) 1.0.0, and Vector 1.0 plus Privilege Specification 1.12 as RISC-V Board formal approval is completed.

For more information, please click here.



Codasip has adopted Imperas reference designs and the Imperas DV solution for Codasip IP.

For more information, please click here.



Imperas RISC-V golden reference models and Verification IP used for functional RISC-V Processor Verification and Architectural Compatibility Testing

For more information, please click here.

Latest Articles

Endless regression: hardware goes virtual on the cloud

In the summer of 2018, professors John Hennessy and David Patterson declared a glorious future for custom hardware. The pair had picked up the Association for Computing Machinery's Turing Award for 2017 for their roles in the development of the reduced instruction set computer (RISC) architectural style in the 1980s.
Towards the end of their acceptance speech, Patterson pointed to the availability of hardware in the cloud as one reason why development of custom chips and the boards they would be soldered onto is getting more accessible. Cloud servers can be used to simulate designs on-demand and, if you have enough dollars to spend, you can simulate a lot of them in parallel to run different tests….

To read the full article by **Chris Edwards**, click here.

ARTICLES FROM SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

Debugging Embedded Applications

Debugging embedded designs is becoming increasingly difficult as the number of observed and possible interactions between hardware and software continue to grow, and as more features are crammed into chips, packages, and systems. But there also appear to be some advances on this front, involving a mix of techniques, including hardware trace, scan chain-based debug, along with better simulation models.
Some of this is due to new tools, some is a combination of existing tools, and some involves a change in methodology in which tools are used in different

combinations at different times in the design-through-manufacturing flow….

To read the full article by **Ann Steffora Mutschler**, click here.

Gaps In The AI Debug Process

When an AI algorithm is deployed in the field and gives an unexpected result, it's often not clear whether that result is correct.
So what happened? Was it wrong? And if so, what caused the error? These are often not simple questions to answer. Moreover, as with all verification problems, the only way to get to the root cause is to break the problem down into manageable pieces.
The semiconductor industry has faced similar problems in the past. Software runs on hardware, and the software must assume the hardware will never make an error. Similarly, when mapping hardware onto an FPGA, it is expected that the FPGA fabric will never make a mistake. In both cases, the underlying execution platforms have been verified to an extent where they built trust over time, and the amount of verification performed on them in some cases is monumental…

To read the full article by **Brian Bailey**, click here.

Product Lifecycle Management For Semiconductors

Product lifecycle management (PLM) and the semiconductor industry have always been separate, but pressure is growing to integrate them. Automotive, IIoT, medical, and other industries see that as the only way to manage many aspects of their business, and as it stands, semiconductors are a large black box in that methodology.
The technology space is driven by a mix of top down and bottom-up processes. Bottom-up tends to be preferred in areas driven by innovation, where being fast and nimble is considered more important than being on time and on budget. Top-down processes are predominant in large systems and industrial development, and they are becoming the preferred way to control products within a company — especially when dealing with large derivative portfolios…

To read the full article by **Brian Bailey**, click here.

Sweeping Changes Ahead For Systems Design

Data centers are undergoing a fundamental change, shifting from standard processing models to more data-centric approaches based upon customized hardware, less movement of data, and more pooling of resources.

Driven by a flood of web searches, Bitcoin mining, video streaming, data centers are in a race to provide the most efficient and fastest processing possible. But because there are so many different types of data, disparities in lifetimes among components, and so much change in software, the magnitude, speed, and breadth of these changes is unprecedented….

To read the full article by **Ann Steffora Mutschler**, click here.

Release Information

riscvOVPsim and riscvOVPsimPlus - LATEST NEWS

The latest Imperas and OVP release at the Open Virtual Platforms website.

For an introduction to RISC-V the free single-core envelope model, called **riscvOVPsim**, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the draft specifications for Bit Manipulation and Vectors.

The latest version was is available via GitHub here.

The free enhanced **riscvOVPsimPlus**, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the OVP website here.

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