Imperas Newsletter – October 2020

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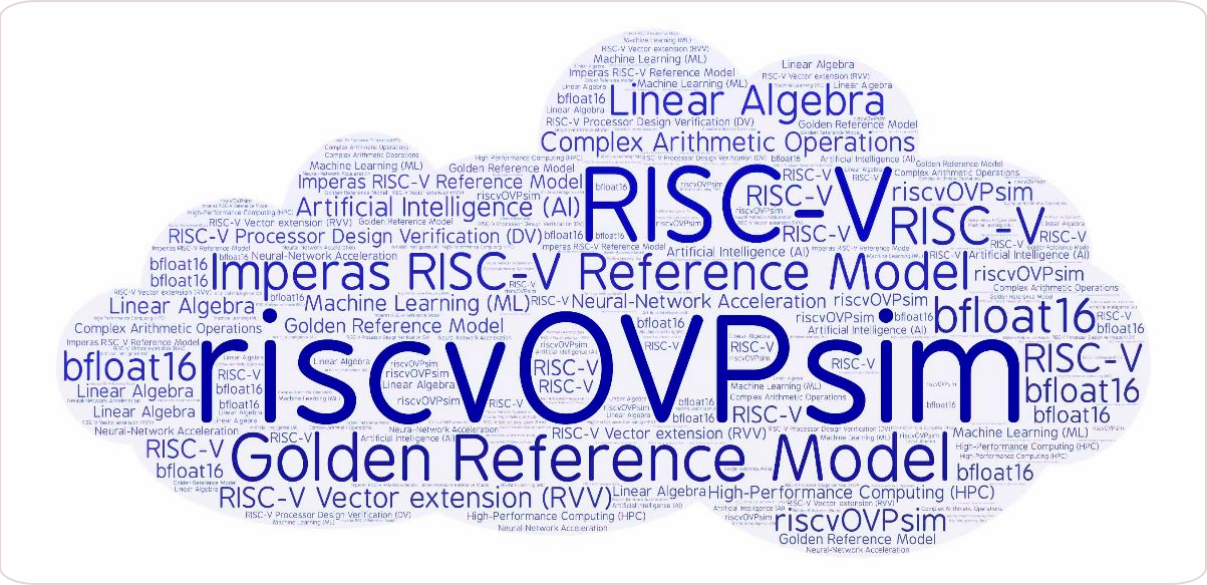
Latest news



riscvOVPsim™ updated for RISC-V Vector Extension Verification

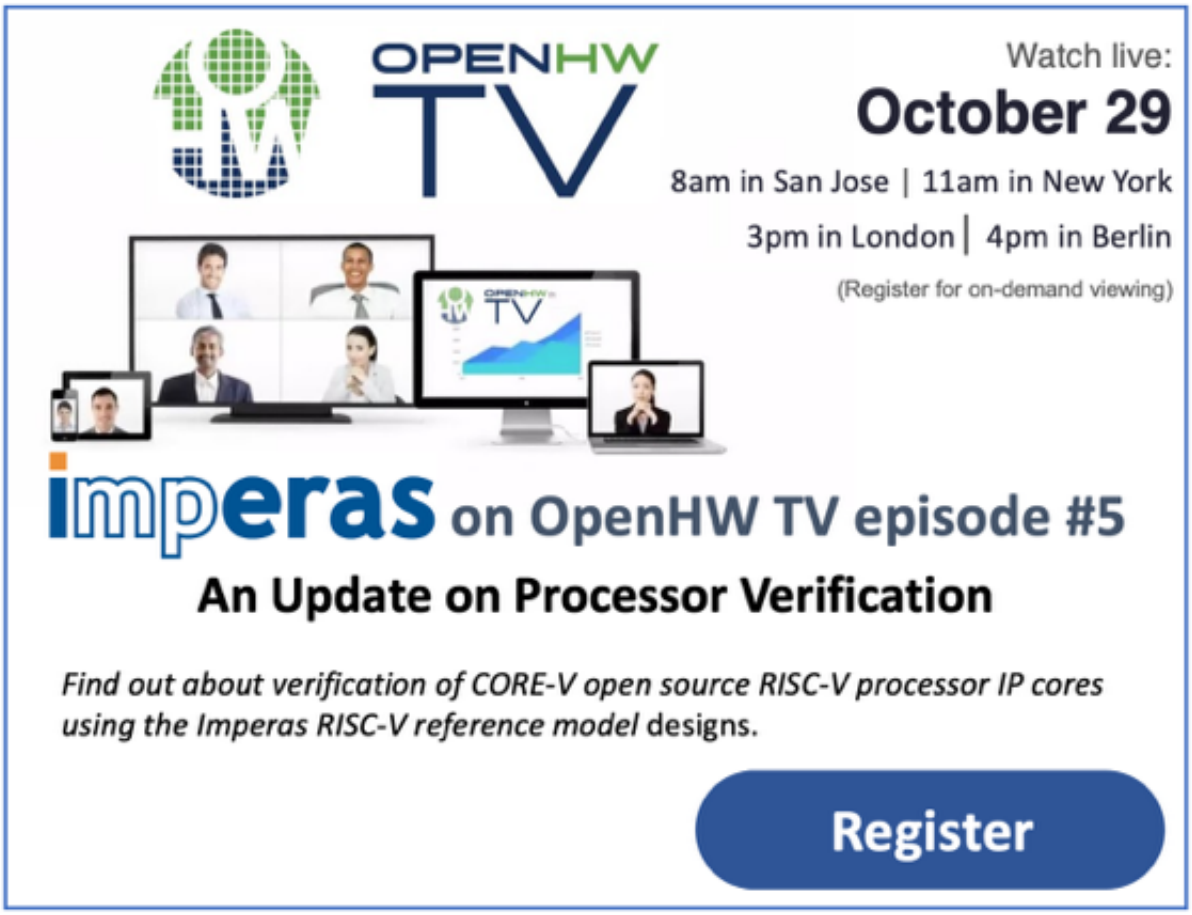
Imperas RISC-V reference simulator and model extended for coverage analysis, plus test suite for latest RISC-V Vector Instruction Extensions

We're excited to announce our free riscvOVPsim™ RISC-V reference model and simulator – which has been widely adopted across the RISC-V ecosystem – has been updated and extended for RISC-V vector extensions with a verification test suite, and now supports coverage driven verification analysis. The base version of riscvOVPsim is available for free from a new GitHub site (github.com/riscv-ovpsim), with an enhanced version including an

extensive RISC-V vector test suite also freely available for commercial use from Open Virtual Platforms (OVPworld.org/riscv-ovpsim).

Read news in full

Events



Join us @ the Embedded Forum

Imperas presentation on: 'Architectural Exploration for AI and Machine Learning – Migrating algorithms to dedicated accelerators in datacenters and edge applications'

Learn more

RISC-V®
Summit

Imperas at 3rd Annual RISC-V Summit

When: 8-10 December 2020

Imperas supporting the online virtual event with the latest updates for RISC-V Processor Verification and Architecture Exploration for AI with virtual platforms.

Register

Recording of webinar on Optimizing RISC-V with Custom Instructions now available

(Event was held on 29 September 2020)

Watch a webinar describing the design flow for adding custom extensions to RISC-V CPU cores to achieve performance gains for accelerators and direct multicore communications for 5G, AI, AR/VR and IoT.

Watch video

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Articles

SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

Divided On System Partitioning

How close can we get to automated system optimization from a software function? The target keeps moving but the tools keep becoming more capable.

BRIAN BAILEY

View the article

Release information

OVP and riscvOVPsim RELEASE NEWS

The latest Imperas and OVP release became available in June 2020, reference 20200630.0. See more details at: http://OVPworld.org/dlp

For an introduction to RISC-V the free single core envelope model, called riscvOVPsim, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the draft specifications for Bit Manipulation and Vectors.

The latest version was uploaded on 21 October 2020, Version: 20201021.0 and is available at: https://github.com/riscv/riscv-ovpsim

The free enhanced riscvOVPsim, including the RISC-V Vector test suite, is now available on OVPworld at https://www.ovpworld.org/riscv-ovpsim

riscvOVPsim, learn more

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