Best bytes from the RISC-V Summit

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RISC-V Reference Model for Processor DV

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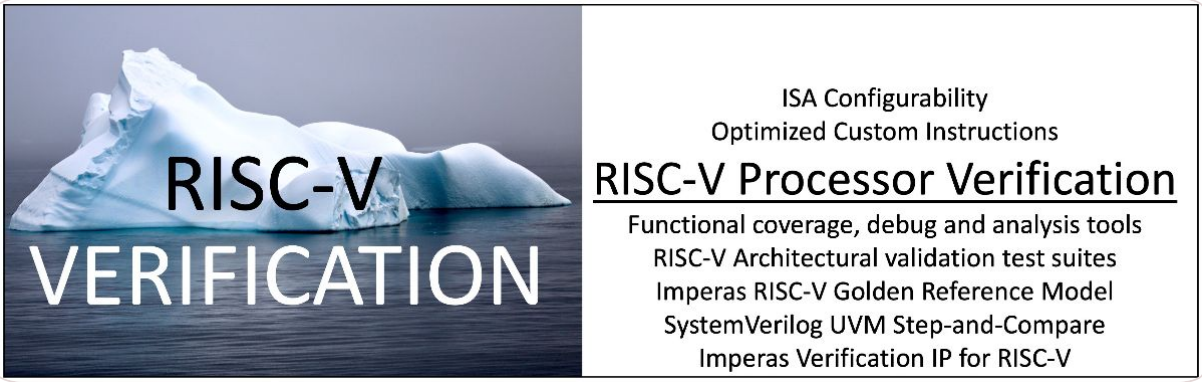


Imperas releases new RISC-V Processor Verification IP

RISC-V adoption boosted with flexible methodology for all SoC adopters

At the RISC-V Summit, we announced that we had made significant enhancements to our RISC-V processor hardware design verification solutions. Our latest release includes an enhanced reference model with SystemVerilog encapsulation / integration and new test bench blocks, new riscvOVPsimPlus™ free simulator, and a range of Imperas developed RISC-V architectural validation tests for the ratified and soon to be ratified RISC-V ISA extensions.

The **free riscvOVPsimPlus RISC-V reference model and simulator**, which has been widely adopted across the RISC-V verification ecosystem, has been updated and extended with additional features including full configurable instruction trace, GDB/Eclipse debug support, plus memory configuration options.

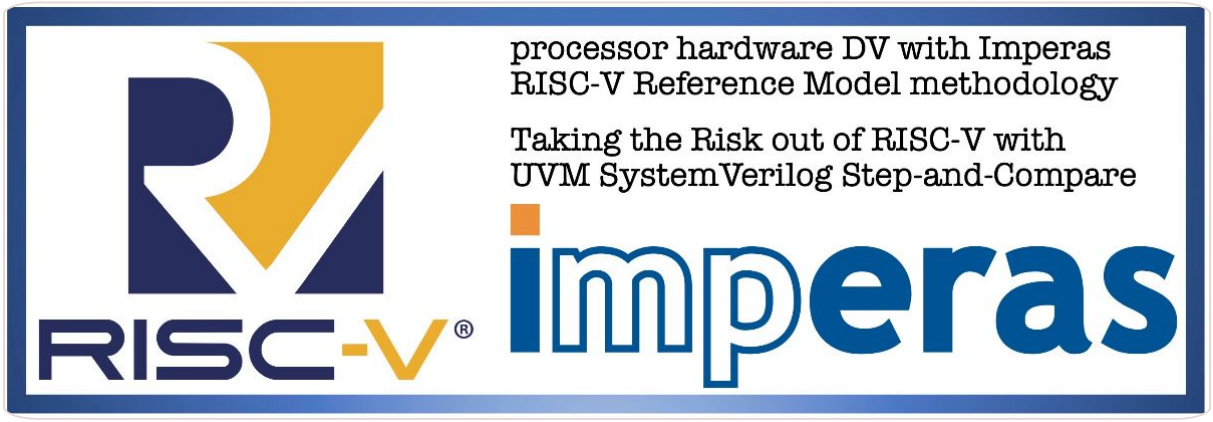
To support the **SystemVerilog encapsulation** of the reference model, the

Imperas RISC-V Processor Verification IP (VIP) package includes example SystemVerilog supporting components and modules for interfacing and synchronization between the Imperas RISC-V golden reference model and the RTL core under test in a step-and-compare verification flow.

To support **instructional and architectural functional coverage**, the Imperas RISC-V golden reference model has been further enhanced with built-in monitors to provide coverage metrics without the need for post-simulation processing or other delays with log file analysis.

Moreover, to help developers ensure their processor design meet the RISC-V specifications, Imperas has developed a directed test instruction generator and is now making many **architectural validation test suites** available.

Read more



Silicon Labs selects Imperas RISC-V Reference Model for verification

SystemVerilog UVM test bench used with step-and-compare between reference and RTL for dynamic testcase scenarios with coverage analysis

Leading the verification activities at the RISC-V Summit, we confirmed the selection by Silicon Labs of the Imperas RISC-V reference model as part of their RISC-V processor verification work.

RISC-V processor verification can be the most complex of tasks within an SoC verification plan and to address the flexibility and configurability of RISC-V it is important that the reference model supports user and privilege modes plus all the standard ratified RISC-V specification variant options. In addition, to support the chip design schedules the reference model also needs to maintain configurability options for all the specification subset references as a dependable golden reference model for verification over the full lifetime of the project design phase and support future software development.

“Silicon Labs selected Imperas simulation tools and RISC-V models for our design verification (DV) flow because of the quality of the models and the ease of use of the Imperas environment,” said **Sebastian Ahmed, Senior Director of R&D at Silicon Labs**. “The Imperas golden reference model of the RISC-V core and their experience with processor RTL DV flows were also critical to our decision.”

“Clear differences exist between many aspects of open-source projects and commercial processor IP, but a common thread in all projects is the desire for adoption and successful implementation in silicon devices,” said **Simon Davidmann, CEO at Imperas Software Ltd.** “Successful implementation for any RISC-V core ultimately relies on the quality of its verification. By including the Imperas RISC-V golden reference model in their advanced SystemVerilog UVM test environment, Silicon Labs can verify their design with confidence.”

Find out more

Imperas extends free-to-use riscvOVPsimPlus Simulator for RISC-V

Latest reference model added and expanded simulation features for debug & trace for early software development and hardware verification

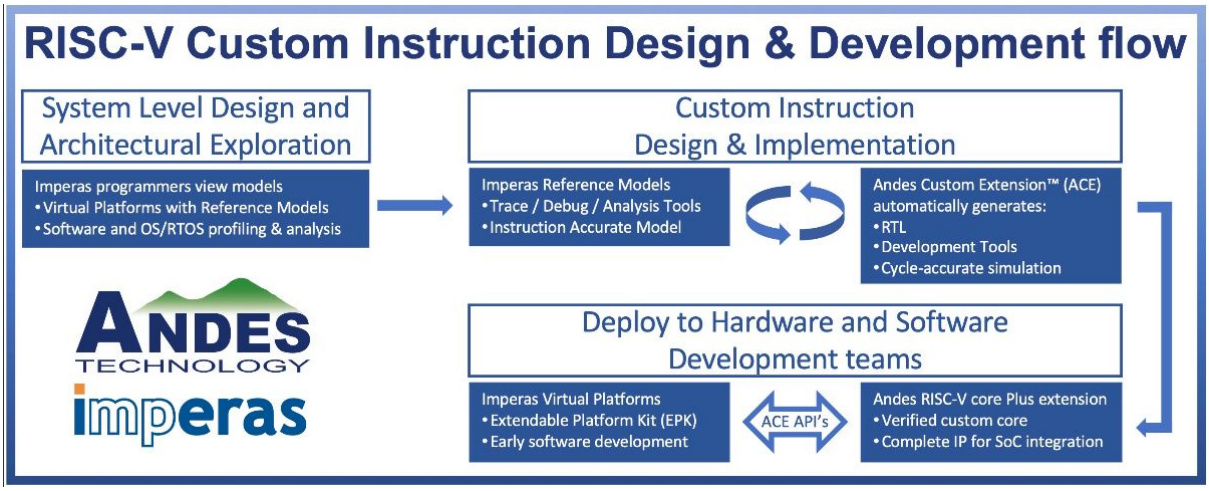
We announced that the free riscvOVPsimPlus™ RISC-V reference model and simulator, which has been widely adopted across the RISC-V ecosystem, has been updated and extended with additional features including full configurable instruction trace, GDB/Eclipse debug support, plus memory configuration options. Additionally, included in the updated model are the full standard CLIC features, Debug Module / Mode, Hypervisor “H” simulation, and also 'near-ratified' ISA extensions for Vector “V”, Bit Manipulation “B”, and Crypto (Scalar) “K” extensions.

riscvOVPsimPlus is an Instruction Accurate RISC-V processor simulator (ISS)

based on the Imperas Open Virtual Platform (OVP) technology with proprietary Just-in-Time Code Morphing simulation technology that executes RISC-V code on a Linux or Windows x86 based host computer. The riscvOVPsimPlus simulator is easy to understand and effective to use. It is flexible, accurate, and exceptionally fast, often over 2,000 MIPS on a modestly configured host machine. It is suitable as a platform target to develop bare metal, OS Ports (Linux or RTOS), driver development as well as full application software.

As a member of the RISC-V community of software, verification and hardware innovators collaboratively driving RISC-V adoption, Imperas has developed the free riscvOVPsimPlus simulator to assist RISC-V adopters to become compliant to the RISC-V specifications. The Imperas RISC-V reference models and simulation technology has been used within RISC-V International's compliance test suite since 2018, and also in verification working groups within CHIPS Alliance and the OpenHW Group.

Learn more



Imperas Simulator Supports Andes Custom Extension to Accelerate Software Development

We've teamed up with Andes Technology Corp., a leading supplier of performance-efficient and extensible 32/64-bit RISC-V CPU cores, to enable SoC design teams using the Andes Custom Extension™ (ACE) framework and Imperas' fast simulators and virtual platforms to co-design hardware and software so that full software development can start before the silicon is available.

Under the ACE framework, SoC designers can easily and efficiently define new instructions on the Andes RISC-V processor core to speed up target applications by writing ACE scripts for instruction semantics and concise Verilog

for instruction execution RTL. Taking them as inputs, the powerful tool COPILOT (Custom-OPtimized Instruction deveLOpment Tools) automatically generates all required components to extend the existing Andes processor package, including the processor RTL, the compilation tools, the debugger and the cycle-accurate simulator, to support the new instructions.

Before the SoC silicon is available for full-speed development, a fast simulator allows software engineers to jump-start the coding, debugging and testing of their applications without depending on the schedule of the hardware development. By taking the extended simulation shared library generated by the COPILOT, the Imperas simulators can automatically recognize the new instructions and simulate their functionality just like a hand-customized simulator. With a fast simulator and the associated tools, software engineers can start full development and even provide feedbacks to hardware designers.

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