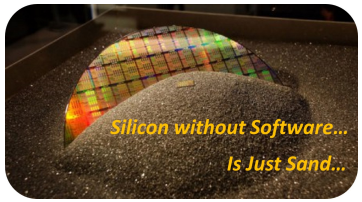
Revolutionizing Embedded Software Development

Imperas Newsletter: September 2017

"Silicon without software is just sand."



New Imperas YouTube Channel

Introducing the new Imperas YouTube channel!
Click here for Imperas on YouTube!

- And please subscribe!

ARM TechCon

Imperas will exhibit and participate in a panel discussion at the 2017 ARM TechCon.

Attend the panel: **"Hypervisors: A Real Trend in Embedded, or Just Hype?"**
Register for a demonstration of Imperas embedded software development, debug and test solutions for ARM-based systems here.

- **Solutions** for custom/proprietary processor modeling, early software development and comprehensive software testing. Use cases include

Sketch Cartoon Introduction to Imperas

This short video uses a cartoon sketch to introduce Imperas.

Five Minutes With... Larry Lapides

Video interview: Five Minutes with Larry Lapides, vice president, Imperas, with Rich Nass, Embedded Computing Design.

Case Study: University of Wrocław Microkernel Development Using MIPS Malta EPK

porting and bring-up of operating systems and hypervisors. See advanced software analysis with Imperas OS-aware verification, analysis and profiling (VAP) tools, code coverage capabilities, memory monitoring, and fault simulation.

- **OVP models and platforms for the full line of ARM processors**, including Cortex-A, R and M families, ARM big.LITTLE architecture and multi-cluster ARMv8 architectures. See Linux booting on various Cortex-A platforms and RTOS booting on Cortex-M platforms.

Read more here.

International System-on-Chip (SoC) Conference

Imperas will participate in the 15th International System-on-Chip Conference, presenting a paper: "RISC-V Models and Simulation Enable Early Software Bring Up." The International System-on-Chip (SoC) Conference is October 18 - 19, 2017 at the University of California, Irvine. The theme for this year's conference is "Secure and Intelligent Silicon Systems for Emerging Applications."
Read more here.

RISC-V Conference

At the University of Wrocław Institute of Computer Science, teams are developing a micro-kernel for the Malta MIPS platform. The project was to investigate the platform and OS development process, learn about internal kernel mechanisms, and explore challenges in designing a micro-kernel. With no access to actual Malta boards, they needed a convenient, affordable solution for high-level simulation and exploration of the Malta platform running OS. Imperas virtual platforms solved the problem!
Read more.

Case Study: Solectrix

Solectrix, with their program for camera-based side-view mirrors for trucks, needed to support ASIL (Automotive Safety Integrity Level) and high safety standards. The application was bare metal software running on the Altera Nios II processor. Testing the binaries was critical for high reliability, so Solectrix used Imperas simulation and OVP Fast Processor Models. Testing actual binaries using Imperas tools allowed the team to find more bugs than with x86 cross compilation. They cited Imperas tools as easy to use; and easy to add into their Agile Continuous Integration (CI) methodology.
Read more.

Korea Automotive Testing Show

Imperas will participate and present high-performance software simulation and virtual platforms at the 7th RISC-V Workshop.
The Imperas session covers virtual prototypes for software development, debug and test. This RISC-V Workshop, hosted by Western Digital in Milpitas California November 28-30 2017, brings the RISC-V community together to share information about RISC-V projects underway around the globe, and build consensus on the evolution of the instruction set.
Read more here.

Imperas Supports Synopsys DesignWare ARCv2 EM Processor Family

Imperas has released virtual platforms and Fast Processor Models for the Synopsys DesignWare ARC EM range of processors, available now, along with software development solutions: simulators, debuggers and other software test and analysis tools. The addition of these ARC models expands existing Imperas and Open Virtual Platforms (OVP) platform support to over 170 processor models across a wide variety of vendors. Also, we will attend the ARC Processor Summit 2017 September 26, in Santa Clara, CA. We hope to see you there!
Read more.

More Events

At the Automotive Technology Expo in Korea, Imperas distribution partner Coontec presented virtual platforms for automotive software debug, test and verification.

Virtual Platform Based Linux Bring Up Methodology: Tutorial slides from DAC 2017

If you missed DAC, you can view the Imperas virtual platform tutorial presentation here: "Linux Bring Up on Heterogeneous Multiprocessor SoCs."
Click here.

- Linley Processor Conference 2017, October 4 - 5, 2017, at the Hyatt Regency, Santa Clara, CA. See Imperas demonstrate virtual platforms for RISC-V designs, at the RISC-V booth. Read more.
- ARC Processor Summit 2017 on Tuesday, September 26, at the Santa Clara Marriott, Santa Clara, CA. Imperas will attend, with news about our ARC IP support!

In the News

- Simon Davidmann interview with Peggy Aycinena in EDA Cafe

OVPsim Release News

OVP: Fast Simulation, Free open source models, Public APIs: Open Virtual Platforms.

A new Imperas and OVP release will be available this month.
The Open Virtual Platforms portal is one of the most exciting open source software developments in the embedded software world since GNU created GDB.

- For embedded software developers, virtual platforms are increasingly important, especially for multi-core designs.

The resources on this portal can significantly accelerate your development and test. The next release of OVPsim is expected to be available in December 2017.